



White Paper
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Intel[®] architecture

Platform Basics

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Executive Summary

Creating an Intel® architecture design encompasses some basic design elements. The configuration and capabilities of these elements can change based on the particular Intel components being supported, but the general concepts apply to all designs. This paper will focus on the implementation of these elements and some considerations for usage based on the type of design being targeted. The elements to be covered are: voltage regulators, clock sources, power sequencing, power states, peripheral I/O interfaces, and general design practices.

The goal of this paper is to describe the basic elements used in building an Intel® architecture design.



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IA Systems

The Intel® architecture (IA) system design is able to utilize some common building block elements that support the Intel devices. Intel provides specifications and standards that enable the industries component suppliers to provide ever increasing levels of integration and performance. The advances in IA performance and capabilities sometimes require updates in the supporting components. This document will go over the key areas of system design and describe the operation of the components in those areas.

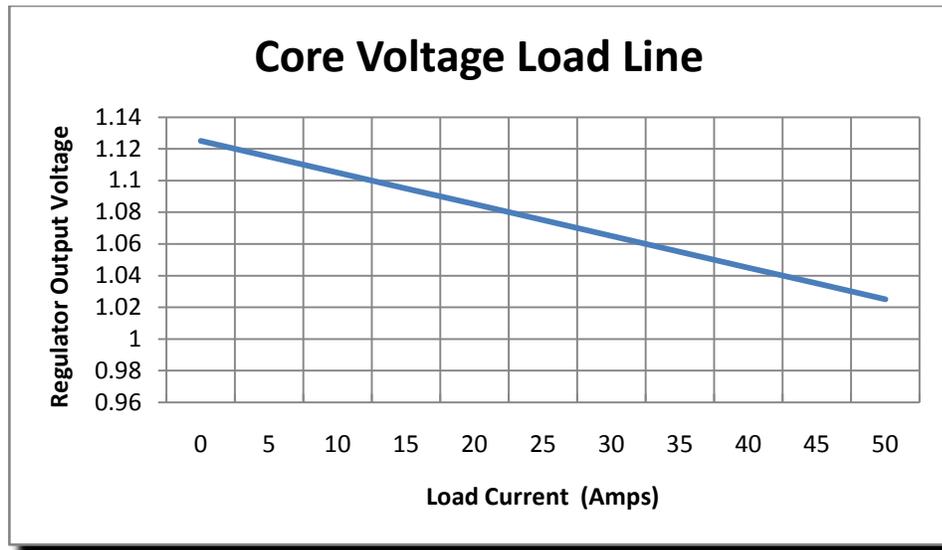
Major Design Areas

Power

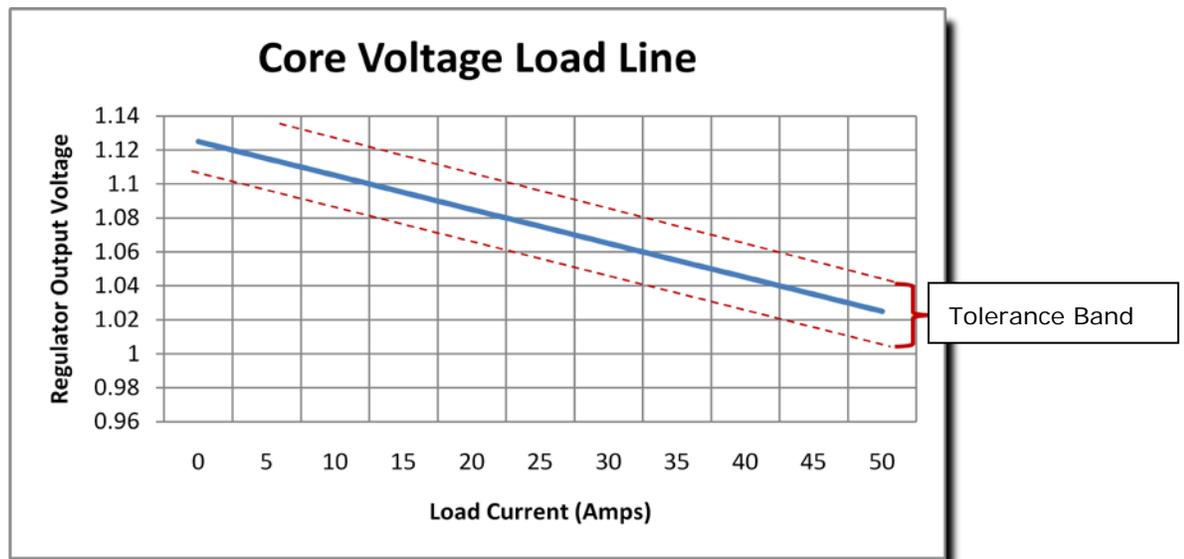
The power needs of the IA design will vary depending on the type of system being built. The Intel components will usually require more than one voltage to maximize the power saving capabilities, as well as staying compatible with I/O voltage standards. Two types of voltage regulators are typically used on IA designs: **switching** and **linear**. The specific Intel component and intended usage will be the primary factors in picking which type of regulator is used. For this document, only the DC voltage realm will be covered.

Switching Regulators

The switching type of regulator is primarily used when power efficiency and current supplying capability are more important to the design than cost and thermal dissipation. The style of switching regulator can also vary greatly based on its usage needs. The most common style of switching regulator in IA designs is the buck or step down regulator. To plan the power delivery strategy of an IA design, the intended usage and modes of support need to be analyzed. If ACPI power states are going to be supported, then some power "rails" will need to be on all the time. If a range of processor versions will be supported, the CPU core voltage regulator may need to support a wider than normal range of loads. The CPU core voltage has special requirements beyond the range of loads. The Intel CPU's core voltage, in most cases, makes use of a load line to specify the regulation and tolerance. The load line defines a slope of voltage with respect to the current required from the regulator. The slope is linear and is specified in the respective EMTS for a given CPU. A common load line slope is 2 milliohm. The current required by the CPU is very dynamic in nature. When the CPU is idling, the current needed will be low, as CPU utilization increases, the current needed will increase.



The “DC” tolerance of the core voltage (the amount of allowable steady noise) is specified as a band of voltage around the load line value (tolerance band).



From an “AC” noise standpoint (transient noise), the load line expectation is that as current demand increases, the allowed voltage output dip is the point on the slope corresponding to the current, minus the tolerance band value.

Many switching power supply controller vendors have worked with Intel to develop their products to meet these operating characteristics. Check with



your preferred vendor to see what is available to meet the Intel load line requirements for your desired CPU.

Another distinction exists between the CPU core voltage regulator and other voltage rails. The CPU has dedicated pins that tell the regulator controller what voltage level to provide. These pins are known as Voltage Identification pins (VID pins). The Intel CPU being used determines how many VIDs will be used and how they are encoded. A standard reference number references these different VID usages in Intel documentation. For desktop and server designs, a VR## nomenclature is used (Voltage Regulator, e.g. VR11, VR11.1). For mobile designs an IMVP # is used (Intel Mobile Voltage Positioning). Embedded designs use both types. Be sure to match up the controller with the specific standard that applies to the CPU used in your design.

Linear Regulators

There are quite a few areas in an IA design that lend themselves to linear regulators. The applicability increases in designs that make use of the standby power modes of the Intel chipsets. There are power rails that require low enough currents to make the linear regulator a suitable choice. In a PC type power design (ATX), the single +5 Volt Standby power rail usually needs to be broken down into much lower voltage rails and linear regulators are commonly used.

Clocking

All IA designs use a basic set of clocks. There are various vendors that supply these basic clocking source devices and Intel works with vendors to ensure that devices are developed to meet the clocking needs of a given CPU. The standard source frequency for these clocking devices is 14.31816MHz and utilizes a clock crystal as the source frequency. A second frequency (32.768 KHz) is needed by IA systems if the time of day needs to be kept. This also uses a clock crystal and normally connects directly to the Intel chipset. If time needs to be kept when the system is powered off, a 3V battery is required by the chipset to maintain the time, and the 32.768 KHz crystal provides the time source.

The system clock source (clock chip) used in a given design needs to meet various specifications of the Intel CPU and chipset, as well as other I/O components in the system. The CPU has pins that connect to the clock chip to program the output frequency of the primary CPU clock (referred to as base clock or BCLK). This allows one design to support multiple CPU versions that may need a different base clock frequency. Since the inclusion of PCI Express* to the Intel chipsets and CPU's, there is also a need for the PCI Express* source clock (100MHz differential) to be provided separately to each PCI Express device in the system. To help facilitate this, the clock chip vendors have developed differential clock buffers that work with the Intel



devices and other I/O devices, specifically meeting the frequency and signal quality that is required.

Another element of the clocking in an IA system is Spread Spectrum Clocking (SSC). The principle of SSC is that the clock chip continually varies its output frequency over a small range (0.5%), centered around the base frequency. The benefit of SSC is realized in the resulting reduction of EMC emissions of the system. Many designs utilize SSC to meet regulatory EMC targets. In most clock chips using SSC is a programmable or strap-able option.

The IA designs using Intel® Xeon® Processors will usually require a specific type of clock chip. In a dual processor system, both CPU's require their own BCLK, and there are typically more I/O devices, so the number of PCIe* source clocks is likely higher. Intel has also worked with the clock chip vendors to develop these types of clock chips.

Sequencing

Sequencing in an IA system typically relates to power supplies, and component control signals. The two primary types of power environments for embedded IA designs are described below.

Power

ATX

The ATX (Advanced Technology Extended) power environment has been developed with direct application into Personal Computer designs. The ATX power standard consists of mechanical and electrical elements and has versions for many system power levels. The basics of the ATX power environment are 4 positive voltages and two negative DC voltage outputs.

- ATX Positive voltages
 - 3.3V
 - 5V
 - 12V
 - 5V Standby
- ATX Negative voltages
 - 5V
 - 12V

The ATX power supply uses AC source power, and when plugged in and turned on it will always have the 5V Standby output energized. An AC switch on the ATX power supply has become common in recent years, so to completely remove the DC voltage outputs, the AC power switch has to be off.

The Intel chipset has accommodations to control the power state of the system and this part of the chipset is powered via the 5V Standby. The



particular voltage level for the chipset will vary, but is nominally between 1.0V and 1.5V. This is a one area where a linear regulator is commonly used to step down the 5V Standby supply. There are a couple of ways for the system to be “awaken” from this standby power state, and the most commonly used one is the power switch. The Intel chipset has a dedicated input pin that can be connected to a mechanical switch, that when activated will start the complete process of turning on and booting up the IA system. The fundamentals of the standby power state and the other intermediate power states are described in the ACPI specifications and will be summarized in another section. The Intel chipset has output signals that should be used to control on board DC power supplies that generate the specific voltage levels needed. Not all Intel chipsets and CPUs use the same voltage levels, so refer to the data sheets and platform design guides for a particular design need for this detail.

The basic sequence of power in the IA system starts with the standby rails, then progresses to chipset and CPU I/O voltages, followed by (or simultaneously) chipset core voltages, then finally the CPU core voltage. It is expected that this sequence is forced by way of “power good” signals from one state to the next. Voltage regulators are commonly available with this power good type of output signal, that becomes active when the regulators output is valid.

The final power good indication is from the CPU core voltage regulator. This power good is used as the final signal to the chipset, to convey that all the power supplies are on and ready.

Combined

In a combined power system, the ATX source supply is not used, and another primary DC voltage comes into the system to provide all the necessary energy. In a combined power system, what normally are standby power rails and main power rails can be combined (when the voltages match). The primary system voltage is usually not at a level that can be directly used by any of the IA components, so step up or down regulators are needed to get all the correct voltages. As with the ATX power mode, there are still sequences for various power rails that need to be met, so power good indications, and other glue logic may be needed to force the proper sequence. In a combined power system, there is usually no use for the Intel chipset power switch input and this can be ignored. When the primary power source is supplied, the system turns on and boots up.

Control Signals

Once the power rails of the IA components are valid, the final power good signal to the chipset lets it de-assert the system and CPU resets signals. At this point the CPU will start a defined process to begin executing instructions from the system BIOS.



Power States

The power states section is relevant to a "PC" like system power architecture. The common usage is for AC power to go to a switching power supply that provides the ATX power rails.

ACPI

Intel platforms have capabilities to optimize power usage. There are multiple standard PC power modes that are documented in the Advanced Configuration and Power Interface (ACPI) specification. It is not the intention of this document to re-iterate all of the ACPI specification, but the global and sleeping states, which affect the platform hardware design, will be highlighted.

Global States

- **G0 (S0)**: System is fully on and running
- **G1, Sleeping States**: (divided into the four states S1 through S4) The behavior of the sleeping state is cumulative as the mode increases (numerically).
 - **S1**: All processor caches are flushed, and the CPU(s) stop executing instructions. Power to the CPU(s) and RAM is maintained; devices that do not indicate they must remain on may be powered down.
 - **S2**: CPU is powered off.
 - **S3**: Commonly referred to as Standby, Sleep, or Suspend to RAM. RAM remains powered, but all non-standby power rails are turned off.
 - **S4**: Hibernation or Suspend to Disk. All content of main memory is saved to non-volatile memory such as a hard drive. The system is powered down to same level as S5.
- **G2 (S5), Soft Off**: G2 is almost the same as G3 Mechanical Off, but some components remain powered so the computer can "wake" from input from the keyboard, clock, LAN, I/O, or USB device.
- **G3, Mechanical Off**: All externally provided power sources are turned off (typically, only the real-time clock is running off its own small internal battery)

System Design

From a system design stand point, a more complicated design will result from the need to support S3 or suspend to RAM. The reason that this can be complicated is that the power source for the system memory voltage needs to be derived from both the main power supply rail and the 5V Standby rail, depending on which mode you are in. The Intel chipset provides control



signals that indicate which ACPI power mode is active, that is the easy part. These signals need to properly control the power circuits so that the voltage that the memory sees is not disrupted when switching to or from S3 mode. The power supply component vendors have developed devices that will properly control the power switching, but make sure that the device you choose can supply the amount of current required by the amount of memory in the system. Refer to the Platform Design Guides for specific recommendations for the CPU/ Chipset that you are using.

I/O

PCI Express*

In the current generation of IA systems, the primary input / output interface is PCI Express. This paper will not go into details about the PCI Express* specification but highlight some design consideration when implementing it. Since the bandwidth of PCI Express* is a direct result of the number of lanes used, the system designer needs to allocate the available lanes according to the bandwidth needs of the device intended. There are considerations when choosing lanes, which relate to the support of lane inversion, polarity inversion, and bifurcation. These can impact the physical implementation of the PCB design. The bifurcation option of Intel components varies, so the datasheet for a device of interest should be referenced. Designing a PCB with PCI Express* needs to follow specific routing rules that are spelled out in the Platform Design Guide associated with the Intel components chosen.

SATA

The Serial Advanced Technology Attachment standard is the prolific method of connection for solid state or rotating data storage. The Intel ICH or PCH devices provide a direct, glueless interface to SATA devices. The family of ICH or PCH will dictate which speed revision of the SATA specification is supported, and all are backward compatible to the original SATA spec. SATA devices are connected through either a cable or a direct connector. The other means of use for SATA is called eSATA or external SATA. The eSATA capability is provided by way of an external (on the end chassis) facing SATA connector. From this connector an externally powered SATA device can be cabled to the system.

USB

The Universal Serial Bus has become very prevalent as the standard external I/O interface for peripherals. The Intel ICH or PCH device provides the USB interface. Designing a USB interface is very straight forward, and there are options provided by ICH or PCH for USB. One option is over-current protection. A 3rd party USB power and protecting device can provide ESD protection and over-current protected power to the USB connector. The ICH



or PCH provides an input for each USB port that accepts status from the protection device so a fault condition can gracefully be dealt with. Another benefit that most ICH or PCH's provide is the ability for a USB device to wake the system from a suspended state (refer to the ACPI section for the suspend state details).

LPC

The LPC (low pin count) interface is a legacy interface that originally replaced a parallel bus on Intel Architecture designs prior to the ICH based architectures. The LPC bus still has some application for lower speed devices. The most common use for the LPC bus is for a Super I/O device (SIO). Various vendors offer SIO's to support legacy interfaces like serial ports, PS/2 mouse and keyboard ports, floppy disk drive, infrared ports, and parallel ports (among others). Some SIO devices also incorporate glue logic that can simplify some power control circuits. Another use for the LPC bus is a Trusted Platform Module (TPM). The TPM is a necessary component when using Intel® Trusted Execution Technology in a design.

SPI

The Serial Peripheral Interface is becoming the prevalent method for connection to the non-volatile memory in a system that stores the BIOS and configuration data. The most common non-volatile memory is Flash EEPROM. The SPI is available on the PCH or ICH and connects directly to a Flash EEPROM device.

Conclusion

Even though the Intel Architecture delivers the most advanced computing platform solutions, the architecting and design of an IA system is relatively straight forward. Though it may sound overused, the Platform Design Guide provides implementation instructions that cover the majority of designs. For the cases where a design is not explicitly covered by the PDG, the datasheets and if needed simulation models are provided to enable a more unique design to be implemented. In addition, the Intel Embedded Design Center website (<http://edc.intel.com>) is a good information reference. The ecosystem of support devices for IA designs is very broad. Power and clocking solutions are available from numerous sources, and in most cases an Intel reference design shows the details for circuit implementations. With the IA at the heart of a design, fantastic products are within reach and are only limited by your imagination.



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Acronyms

ACPI Advanced Configuration and Power Interface

BIOS Basic Input Output System

CPU Central Processing Unit

EMTS Electro-Mechanical Thermal Specification

IA Intel® architecture

ICH Input / Output Control Hub

PCH Platform Control Hub

PDG Platform Design Guide

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