Solution Brief

Telecommunications
Intel FPGAs

SmartNICs with Intel® FPGAs Boost Performance for Converged Broadband Networks

FPGA-based SmartNICs can help transform wireless and wireline broadband access networks by accelerating hardware performance and improving scalability in a cost-effective way.

Delivering broadband Internet is expensive, particularly for telecommunications service providers (telcos) who offer both wireless and wireline access to customers. These providers rely on a complex, dual infrastructure that they must constantly upgrade and maintain at great cost to meet consumer demands. Given these high expenses, telco Internet providers are exploring new ways of reducing costs and creating new revenue streams. Many operators, for example, are eyeing 5G fixed-mobile convergence (FMC) as a way to converge mobile and broadband network infrastructure, lower costs, and add new agile services. FMC also helps meet the needs of consumers and businesses that are looking for multi-access connectivity and a seamless service experience.

Infrastructure innovations raise hopes for new revenue streams

Recent innovations are supporting the goal of hosting and delivering new services through a consolidated, less-expensive infrastructure. For example, the Access Gateway Function (AGF) is a key FMC component that enables wireless-wireline convergence and that integrates and interoperates with the 5G core network through a variety of deployment options. Other innovations, such as software-defined networking (SDN) and network function virtualization (NFV), are key to enabling the network transformation at the telco's edge to support the User Plane Function (UPF), AGF, and Broadband Network Gateway (BNG). The combination of these new capabilities enables higher throughput and lower latency for traffic between the telco central office (CO) and all their broadband customers, both wireless and wireline, through a newly shared infrastructure. A map of this simplified architecture is shown in Figure 1.

Wanted: a scalable, cost-effective hardware solution to support fixed-mobile convergence

Despite these exciting innovations, finding the right hardware on which to host these new virtual network functions (VNFs) at the network edge is a big challenge. Telco central offices (COs) have limited physical space with constraints on power and cooling. The hardware solution also needs to be cost-effective enough to support the goals of reduced capital expenditures (CapEx) and operating expenses (OpEx). Finally, the solution needs to enable low-latency services and scale well enough to handle tens of thousands—or even hundreds of thousands—of subscriber connections.

FPGA-based SmartNICs deliver cost-effective scalability

SmartNICs built with Intel FPGAs provide a solution to this hardware problem while still offering the advantages of a commercial off-the-shelf (COTS) solution. Intel FPGA-based SmartNICs can be used to accelerate the UPF, AGF, and BNG, including key features such as high-throughput packet processing, smart and effective

> **"As a leading provider of connectivity solutions, it's clear that SmartNICs can dramatically improve the performance and efficiency of 4G/5G edge deployments for Telco providers," said Boris Beletsky, AVP, Emerging Technologies. "The Silicom FPGA SmartNIC N5010 is the first hardware programmable 4x100GbE FPGA accelerated SmartNIC that enables next generation IA-based servers to meet the performance and scaling needs of the 5G core network (UPF), access gateways (BNG, AGF), and security functions (Firewall, IPsec)."**

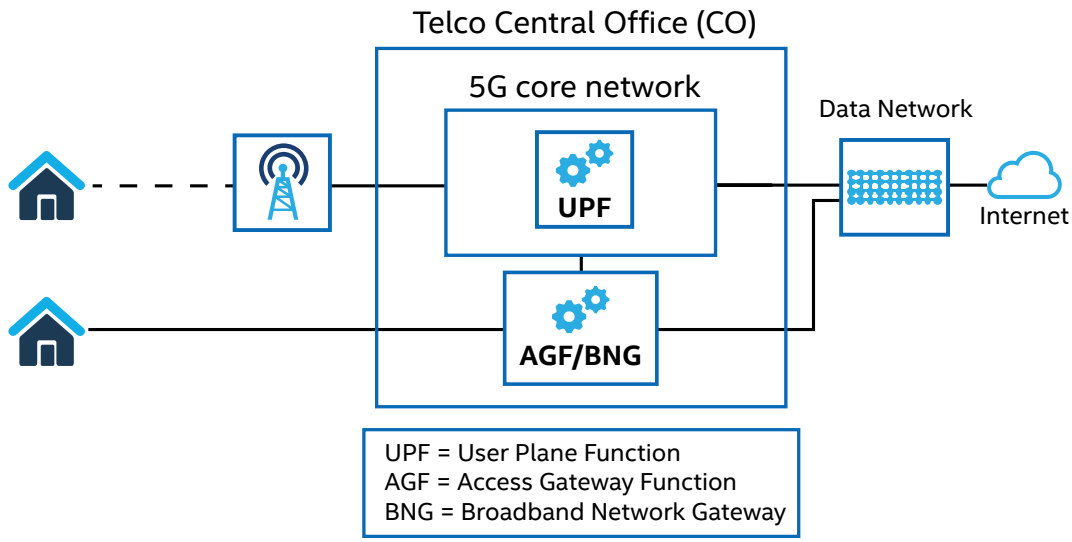

Figure 1. Recent innovations in telecommunications architecture help enable the delivery of premium, telco-hosted services to both wireless and wireline customers

packet load balancing to CPU cores, and Hierarchical Quality of Service (HQoS). These capabilities are crucial to support high bandwidth and low latency in a converged access network.

Operators can use Intel FPGA-based SmartNICs to accelerate different hardware solutions for VNFs, based on performance requirements and the population density of the area served. For example, a COTS server accelerated by an Intel FPGA-based SmartNIC can be used to cost-effectively host a UPF, AGF, and BNG with high performance in regions with medium population density. In densely populated regions with more subscribers, Intel FPGA-based SmartNICs in COTS servers can be used in conjunction with a white box switch powered by an Intel® Tofino™ application-specific integrated circuit (ASIC) chip to host terabit-level, P4-programmable UPF, AGF, and BNG components.

Intel® Stratix® FPGAs power high-performance SmartNICs

Silicom, among other vendors, offers SmartNICs that are built with Intel Stratix 10 FPGAs. These SmartNICs are high-performance acceleration cards that can be optimized to process packets and manage traffic for the AGF, BNG, and UPF. The Silicom SmartNICs accelerate these VNFs by offloading packet parsing and classification, stateful load balancing, and HQoS from the x86-based CPU. For example, the Silicom FPGA SmartNIC N5010 can support multi-100Gbps (up to 400Gbps) HQoS with more than 100,000 queues.

Accelerated components and features for telecommunications

Intel FPGA–based SmartNICs can be used to accelerate a wide variety of functions in a telecommunications infrastructure. These devices support current-generation wireline and 4G wireless functions, and they are now being updated to support next-generation wireline and 5G wireless functions. More specifically, the following workloads can be accelerated by FPGA-based SmartNICs available from Intel and third parties such as Silicom:

Silicom FPGA SmartNIC N5010

The Silicom FPGA SmartNIC N5010 is a high-performance, programmable PCIe server adapter featuring an Intel Stratix DX210 FPGA. It is designed to accelerate various applications and features in a telecommunications infrastructure, such as network functions, security features, and telemetry features.

Key hardware features of the Silicom FPGA SmartNIC N5010:

- Intel Stratix 10 FPGA
- Intel Ethernet Controller E810
- High-speed network interface support: 4x100 Gigabit Ethernet (GbE) and 4x4x25 GbE
- 2 x PCIe x16 Gen 4 (16 physical)
- Low-latency memory access: 32 GB DDR4 memory, 144 MB QDR4, 8 GB high-bandwidth memory (HBM) (2 x 4 GB/stack)

See the section "Accelerated components and features for telecommunications" in this paper for more information about the telecommunications components and features that can be accelerated by the Silicom FPGA SmartNIC N5010.

Network functions:

- 4G Virtual Evolved Packet Core (vEPC)
- 5G UPF, 5G AGF[1]
- Virtual Broadband Network Gateway (vBNG)
- Segment Routing over IPv6 (SRv6)
- Carrier-Grade Network Address Translation (CGNAT)

(List continues on next page)

Network security and telemetry:

- Virtual firewall (vFW)
- IP Security (IPsec)
- Transport Layer Security (TLS)
- Packet monitoring and analytics

FPGAs help ensure flexibility and agility

Because Intel FPGAs can be reprogrammed and orchestrated in the field, FPGA-based SmartNICs give communication service providers (CoSPs) the flexibility to deliver new features and adapt to evolving needs. Reprogramming the SmartNIC is enabled by the open-source Data Plane Development Kit (DPDK) driver, the Open Programmable Acceleration Engine (OPAE), and the P4 programming language. The DPDK driver provides an interface to offload certain DPDK-based modules to the SmartNIC. OPAE, meanwhile, is the API used to access and manage FPGAs.

Intel FPGA–based SmartNICs deliver the performance needed in a modern telecom infrastructure, at an affordable price

By accelerating VNFs at the network edge, Intel and Silicom SmartNICs can help transform broadband delivery for telcos. These providers can use Intel FPGA-based SmartNICs to reduce infrastructure complexity, CapEx, and OpEx while improving performance and scalability. Finally, with the help of this technology, telcos can modernize their broadband infrastructure and deliver real-time, high-performance services that bring in new revenue streams.

Learn More

For more information about Intel FPGA–based SmartNICs, visit: **intel.com/content/www/us/en/programmable/solutions/acceleration-hub/platforms.html**.

For more information about Intel FPGAs, visit: **intel.com/content/www/us/en/programmable/solutions/acceleration-hub/solutions.html**.

[1] AGF and UPF features available soon.

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