Intel® Solid State Drive 540s Series (M.2)

Product Specification

- Capacities: 120, 180, 240, 360, 480, 1000 GB
- Form Factors:
  - 80mm (single-sided) 2280-S3-B-M (120, 180, 240, 360, 480 GB)
  - 80mm (double-sided) 2280-D3-B-M (1000 GB)
- Thickness: S3 – up to 2.38 mm; D3 – up to 3.73 mm
- Weight: <7 grams
- SATA 6Gb/s Bandwidth Performance\(^1\,^2\)
  (IOMeter\(^*\) Queue Depth 32)
  - Sequential Read: up to 560MB/s
  - Sequential Write: up to 480MB/s
- Read and Write IOPS\(^1\,^2\)
  (IOMeter Queue Depth 32)
  - Random 4KB Reads: up to 78,000 IOPS
  - Random 4KB Writes: up to 85,000 IOPS
- Additional Compatibility
  - Intel® SSD Toolbox with Intel® SSD Optimizer
  - Intel® Data Migration Software
  - Intel® Rapid Storage Technology
  - SATA Revision 3.2
  - ACS-3 (ATA/ATAPI Command Set 3)
  - SSD Enhanced SMART ATA feature set
- AES 256-bit Encryption
- Power Management
  - 3.3 V SATA Supply Rail
  - SATA Link Power Management (LPM)
  - Device Sleep (DevSleep)
  - Advanced Power Management (APM)
- Power
  - Active (BAPCo MobileMark\(^*\) 2012 Workload): 80 mW
  - Idle\(^3\): 40 mW
  - DevSleep: 3 mW
- Temperature
  - Operating: 0° C to 70° C
  - Non-Operating: -55° C to 95° C
- Reliability
  - Uncorrectable Bit Error Rate (UBER): <1 sector per 10\(^{16}\) bits read
  - Mean Time Between Failure (MTBF): 1.6 million hours
  - Shock (non-operating): 1,000 G/0.5 ms
- Vibration
  - Operating: 2.17 GRMS (5-700Hz)
  - Non-operating: 3.13 GRMS (5-800Hz)
- Certifications and Declarations:
  - UL\(^*\)
  - CE\(^*\)
  - RCM\(^*\)
  - BSMI\(^*\)
  - KCC\(^*\)
  - Microsoft\(^*\) WHCK/WHLK
  - VCCI\(^*\)
  - SATA-IO\(^*\)
- Product Ecological Compliance
  - RoHS\(^*\)

NOTES:
2. Performance values vary by capacity.
3. Non-DevSleep idle power with SATA Link Power Management (LPM) enabled.
4. As measured by temperature sensor, SMART Attribute BEh. Active airflow is recommended within the system for maintaining proper device operating temperatures on heavier workloads.

Order Number: 334047-001US
Ordering Information

Contact your local Intel sales representative for ordering information.

Revision History

<table>
<thead>
<tr>
<th>Revision Number</th>
<th>Description</th>
<th>Revision Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>Initial release</td>
<td>March 2016</td>
</tr>
</tbody>
</table>

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase.


All documented test results are obtained by Intel in compliance with JESD218 Standards; refer to individual sub-sections within this document for specific methodologies. See www.jedec.org for detailed definitions of JESD218 Standards.

Low Halogen applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components on the finished assembly meet JS-709 requirements, and the PCB/substrate meet IEC 61249-2-21 requirements.

The replacement of halogenated flame retardants and/or PVC may not be better for the environment.

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The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order. This document contains information on products in the design phase of development.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to: http://www.intel.com/design/literature.htm

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1 Introduction

This document describes the specifications and capabilities of the Intel® Solid State Drive 540s Series (Intel® SSD 540s Series).

1.1 Terminology

Table 1: Terminology

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AHCI*</td>
<td>Advanced Host Controller Interface</td>
</tr>
<tr>
<td>ATA</td>
<td>Advanced Technology Attachment</td>
</tr>
<tr>
<td>DAS</td>
<td>Device Activity Signal</td>
</tr>
<tr>
<td>DevSleep</td>
<td>Device Sleep</td>
</tr>
<tr>
<td>DIPM</td>
<td>Device Initiated Power Management</td>
</tr>
<tr>
<td>DMA</td>
<td>Direct Memory Access</td>
</tr>
<tr>
<td>DPTF</td>
<td>Dynamic Platform Thermal Framework</td>
</tr>
<tr>
<td>EXT</td>
<td>Extended</td>
</tr>
<tr>
<td>FPDMA</td>
<td>First Party Direct Memory Access</td>
</tr>
</tbody>
</table>
| GB | Gigabyte (1,000,000,000 bytes)  
Note: The total usable capacity of the SSD may be less than the total physical capacity because a small portion of the capacity is used for NAND flash management and maintenance purposes. |
<p>| HDD | Hard Disk Drive |
| HIPM | Host Initiated Power Management |
| I/O | Input/Output |
| IOPS | Input/Output Operations Per Second |
| KB | Kilobyte (1,024 bytes) |
| LBA | Logical Block Address |
| LPM | Link Power Management |
| MB | Megabyte (1,000,000 bytes) |
| MLC | Multi-level Cell |
| MTBF | Mean Time Between Failures |
| NCQ | Native Command Queuing |
| NOP | No Operation |
| PIO | Programmed Input/Output |
| RDT | Reliability Demonstration Test |
| RMS | Root Mean Squared |
| SLC | Single-level Cell |
| SATA | Serial Advanced Technology Attachment |</p>
<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMART</td>
<td>Self-Monitoring, Analysis and Reporting Technology</td>
</tr>
<tr>
<td>SSD</td>
<td>Solid State Drive</td>
</tr>
<tr>
<td>TYP</td>
<td>Typical</td>
</tr>
<tr>
<td>UBER</td>
<td>Uncorrectable Bit Error Rate</td>
</tr>
</tbody>
</table>

### 1.2 Reference Documents

Table 2: Standard References

<table>
<thead>
<tr>
<th>Date or Rev. #</th>
<th>Title</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dec 2008</td>
<td>VCCI</td>
<td><a href="http://www.vcci.jp/vcci_e/">http://www.vcci.jp/vcci_e/</a></td>
</tr>
<tr>
<td>June 2009</td>
<td>RoHS</td>
<td><a href="http://qdms.intel.com/">http://qdms.intel.com/</a> Click Search MDDS Database and search for material description datasheet</td>
</tr>
<tr>
<td>August 2013</td>
<td>Serial ATA Revision 3.2</td>
<td><a href="http://www.sata-io.org/">http://www.sata-io.org/</a></td>
</tr>
</tbody>
</table>
## 2 Product Specifications

### 2.1 Capacity

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Unformatted Capacity (Total User Addressable Sectors in LBA mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td>120GB</td>
<td>234,441,648</td>
</tr>
<tr>
<td>180GB</td>
<td>351,651,888</td>
</tr>
<tr>
<td>240GB</td>
<td>468,862,128</td>
</tr>
<tr>
<td>360GB</td>
<td>703,282,608</td>
</tr>
<tr>
<td>480GB</td>
<td>937,703,088</td>
</tr>
<tr>
<td>1000GB</td>
<td>1,953,525,168</td>
</tr>
</tbody>
</table>

### 2.2 Performance

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Random 4KB Read (up to)¹</th>
<th>Random 4KB Write (up to)¹</th>
<th>Sequential 128KB Read¹</th>
<th>Sequential 128KB Write¹</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IOPS</td>
<td>IOPS</td>
<td>MB/s</td>
<td>MB/s</td>
</tr>
<tr>
<td>120GB</td>
<td>60,000</td>
<td>50,000</td>
<td>560</td>
<td>400</td>
</tr>
<tr>
<td>180GB</td>
<td>71,000</td>
<td>85,000</td>
<td>560</td>
<td>475</td>
</tr>
<tr>
<td>240GB</td>
<td>74,000</td>
<td>85,000</td>
<td>560</td>
<td>480</td>
</tr>
<tr>
<td>360GB</td>
<td>74,000</td>
<td>85,000</td>
<td>560</td>
<td>480</td>
</tr>
<tr>
<td>480GB</td>
<td>78,000</td>
<td>85,000</td>
<td>560</td>
<td>480</td>
</tr>
<tr>
<td>1000GB</td>
<td>78,000</td>
<td>85,000</td>
<td>560</td>
<td>480</td>
</tr>
</tbody>
</table>

Note:
1. Performance measured within the SLC cache buffer using IOMeter* with Queue Depth 32.

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Random 4KB Read (up to)¹</th>
<th>Random 4KB Write (up to)¹</th>
<th>Sequential 128KB Read¹</th>
<th>Sequential 128KB Write¹</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IOPS</td>
<td>IOPS</td>
<td>MB/s</td>
<td>MB/s</td>
</tr>
<tr>
<td>120GB</td>
<td>55,000</td>
<td>13,500</td>
<td>560</td>
<td>70</td>
</tr>
<tr>
<td>180GB</td>
<td>65,000</td>
<td>22,000</td>
<td>560</td>
<td>90</td>
</tr>
<tr>
<td>240GB</td>
<td>70,000</td>
<td>29,000</td>
<td>560</td>
<td>100</td>
</tr>
<tr>
<td>360GB</td>
<td>70,000</td>
<td>29,000</td>
<td>560</td>
<td>100</td>
</tr>
<tr>
<td>480GB</td>
<td>72,000</td>
<td>36,000</td>
<td>560</td>
<td>125</td>
</tr>
<tr>
<td>1000GB</td>
<td>72,000</td>
<td>36,000</td>
<td>560</td>
<td>125</td>
</tr>
</tbody>
</table>

Note:
1. Performance measured using IOMeter* with Queue Depth 32. Measurements are performed on 8GB of Logical Block Address (LBA) range on a full SSD.
**Table 6: Latency**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Intel® SSD 540s Series Type 2280</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read¹</td>
<td>50 µs (TYP)</td>
</tr>
<tr>
<td>Write¹</td>
<td>60 µs (TYP)</td>
</tr>
<tr>
<td>Power On To Ready²</td>
<td>500 ms (TYP)</td>
</tr>
<tr>
<td>Max Power On To Ready³</td>
<td>&lt; 10 sec</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Based on sequential 4KB using IOMeter with Queue Depth 1 workload. Write Cache enabled.
2. Power On To Ready time assumes safe shutdown
3. Max Power On To Ready time assumes unsafe shutdown. Based on statistical measurement of 95% quality of service.

### 2.3 Electrical Characteristics

**Table 7: Operating Voltage and Power Consumption**

<table>
<thead>
<tr>
<th>Electrical Characteristics</th>
<th>Intel® SSD 540s Series Type 2280</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>120GB</td>
</tr>
<tr>
<td>Operating Voltage for 3.3 V (±5%)</td>
<td></td>
</tr>
<tr>
<td>Min</td>
<td>3.14 V</td>
</tr>
<tr>
<td>Max</td>
<td>3.47 V</td>
</tr>
<tr>
<td>Rise Time (Max/Min)</td>
<td>100 ms / 0.1 ms</td>
</tr>
<tr>
<td>Fall Time (Max/Min)</td>
<td>5 s / 1 ms</td>
</tr>
<tr>
<td>Noise Tolerance</td>
<td>70 mV pp (10 Hz – 30 MHz)</td>
</tr>
<tr>
<td>Min Off Time¹</td>
<td>1 s</td>
</tr>
<tr>
<td>Power Consumption (TYP)</td>
<td></td>
</tr>
<tr>
<td>Active²</td>
<td>80 mW</td>
</tr>
<tr>
<td>Idle³</td>
<td>40 mW</td>
</tr>
<tr>
<td>DevSleep⁴</td>
<td>3 mW</td>
</tr>
<tr>
<td>Thermal Power⁵</td>
<td></td>
</tr>
<tr>
<td>Regulator Power⁶</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Minimum time from when power removed from drive (Vcc < 100 mV) to when power can be reapplied to drive.
2. Active power measured during execution of MobileMark* 2012 with SATA Link Power Management (LPM) enabled.
3. Non-DevSleep idle power with SATA Link Power Management (LPM) enabled.
4. Power consumption during DevSleep state.
5. Power measured during 128kB sequential writes with Queue Depth 32 workload using 100 ms sample period. This represents power that would be thermal load on system during heavy workloads.
6. Power measured during 128kB sequential writes with Queue Depth 32 workload using 500 us sample period. This represents power that system power supply would have to regulate for proper device operation.
2.4 Environmental Conditions

2.4.1 Temperature, Shock, Vibration

Table 8: Temperature, Shock, Vibration

<table>
<thead>
<tr>
<th>Electrical Characteristics</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module Temperature</td>
<td></td>
</tr>
<tr>
<td>Operating$^1$</td>
<td>0° C – 70° C</td>
</tr>
<tr>
<td>Non-operating$^2$</td>
<td>-55° C – 95° C</td>
</tr>
<tr>
<td>Temperature Gradient$^3$</td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>30 (TYP)$^a$ C/hr</td>
</tr>
<tr>
<td>Non-operating</td>
<td>30 (TYP)$^a$ C/hr</td>
</tr>
<tr>
<td>Humidity</td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>5 – 95 %</td>
</tr>
<tr>
<td>Non-operating</td>
<td>5 – 95 %</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Shock and Vibration</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shock$^4$</td>
<td></td>
</tr>
<tr>
<td>Non-operating</td>
<td>1,000 G (Max) at 0.5 msec</td>
</tr>
<tr>
<td>Vibration$^5$</td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>2.17 GRMS (5-700 Hz) Max</td>
</tr>
<tr>
<td>Non-operating</td>
<td>3.13 GRMS (5-800 Hz) Max</td>
</tr>
</tbody>
</table>

NOTES:
1. As measured by temperature sensor, SMART Attribute BEh. Active airflow is recommended within the system for maintaining proper device operating temperature on heavier workloads.
2. Please contact your Intel representative for details on the non-operating temperature range.
3. Temperature gradient measured without condensation.
4. Shock specifications assume SSD is mounted securely with the input vibration applied to the drive-mounting screws. Stimulus may be applied in the X, Y or Z axis. Shock specification is measured using peak acceleration and pulse width value.
5. Vibration specifications assume the SSD is mounted securely with the input vibration applied to the drive-mounting screws. Stimulus may be applied in the X, Y or Z axis. Vibration specification is measured using G Root Mean Squared (GRMS) value.

2.4.2 Altitude

The drive is not sensitive to changes in atmospheric pressure because it has no moving parts. Drive tested under non-operational conditions to pressures representative of -1 K and +40 K feet.

2.5 Product Regulatory Compliance

The Intel SSD 540s Series meets or exceeds the regulatory or certification requirements as specified in the Intel SSD 540s Series Declaration of Conformity at http://www.intel.com/content/www/us/en/library/tech-docs.results.html?mTag=rresourceType:technicaldocument/declarationofconformity
2.6 Reliability

The Intel SSD 540s Series meets or exceeds SSD endurance and data retention requirements as specified in the JESD218 specification.

Table 9: Reliability Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncorrectable Bit Error Rate (UBER)</td>
<td>&lt; 1 sector per $10^{16}$ bits read</td>
</tr>
<tr>
<td>Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In the unlikely event of a non-recoverable read error, the SSD will report it as a read failure to the host; the sector in error is considered corrupt and is not returned to the host.</td>
<td></td>
</tr>
<tr>
<td>Mean Time Between Failures (MTBF)</td>
<td>≥ 1.6 million hours</td>
</tr>
<tr>
<td>Mean Time Between Failures is estimated based on Telcordia* methodology and demonstrated through Reliability Demonstration Test (RDT).</td>
<td></td>
</tr>
<tr>
<td>Minimum Useful Life/Endurance Rating</td>
<td>5 years</td>
</tr>
<tr>
<td>The SSD will have a minimum of five years of useful life under typical client workloads with up to 40 GB of host writes per day.</td>
<td></td>
</tr>
<tr>
<td>Insertion Cycles</td>
<td>250 insertion/removal cycles on M.2 port</td>
</tr>
</tbody>
</table>

*120GB SSD qualified to 20 GB of host writes per day.
3 Mechanical Information

The following figures show the mechanical information for the single-sided, 80 mm height, M.2 Intel SSD 540s Series. All dimensions are in millimeters.

Figure 1: Dimensions for 80 mm single-sided M.2 Form Factor Drives (2280-S3-B-M)
Figure 2: Dimensions for 80 mm double-sided M.2 Form Factor Drives (2280-D3-B-M)
4 Pin and Signal Descriptions

4.1 Pin Locations

Figure 3: Layout of Signal and Power Segment Pins
## 4.2 Signal Descriptions

Table 10: M.2 Serial ATA Power Pin Definitions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>CONFIG_3</td>
<td>Ground</td>
</tr>
<tr>
<td>P2</td>
<td>+3.3 V</td>
<td>3.3 V Source</td>
</tr>
<tr>
<td>P3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P4</td>
<td>+3.3 V</td>
<td>3.3 V Source</td>
</tr>
<tr>
<td>P5</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P6</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P7</td>
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<tr>
<td>P8</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P9</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P10</td>
<td>DAS/DSS#</td>
<td>Device Activity Signal / Disable Staggered Spin-up</td>
</tr>
<tr>
<td>P11</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P12</td>
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<td>No Connect</td>
</tr>
<tr>
<td>P13</td>
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</tr>
<tr>
<td>P14</td>
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<td>No Connect</td>
</tr>
<tr>
<td>P15</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P16</td>
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<td>No Connect</td>
</tr>
<tr>
<td>P17</td>
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<td>No Connect</td>
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<td>P18</td>
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<td>No Connect</td>
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<tr>
<td>P19</td>
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<tr>
<td>P20</td>
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<td>No Connect</td>
</tr>
<tr>
<td>P21</td>
<td>CONFIG_0</td>
<td>Ground</td>
</tr>
<tr>
<td>P22</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P23</td>
<td>Reserved</td>
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<td>Reserved</td>
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<tr>
<td>P26</td>
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<td>P27</td>
<td>GND</td>
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<tr>
<td>P29</td>
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<td>No Connect</td>
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<tr>
<td>P30</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P31</td>
<td>Reserved</td>
<td>No Connect</td>
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<td>P32</td>
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<td>P34</td>
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<td>P35</td>
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<tr>
<td>P36</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P37</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P38</td>
<td>DEVSLEEP</td>
<td>DevSleep Pin</td>
</tr>
<tr>
<td>P39</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P40</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P41</td>
<td>+B</td>
<td>Host Receiver Differential Signal Pair (This is an output of the SSD)</td>
</tr>
<tr>
<td>P42</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P43</td>
<td>-B</td>
<td>Host Receiver Differential Signal Pair (This is an output of the SSD)</td>
</tr>
<tr>
<td>Pin</td>
<td>Function</td>
<td>Definition</td>
</tr>
<tr>
<td>-----</td>
<td>----------------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>P44</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P45</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P46</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P47</td>
<td>-A</td>
<td>Host Transmitter Differential Signal Pair (This is an input of the SSD)</td>
</tr>
<tr>
<td>P48</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P49</td>
<td>+A</td>
<td>Host Transmitter Differential Signal Pair (This is an input of the SSD)</td>
</tr>
<tr>
<td>P50</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P51</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P52</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P53</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P54</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P55</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P56</td>
<td>Two Wire Interface</td>
<td>Two Wire Interface Clock</td>
</tr>
<tr>
<td>P57</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P58</td>
<td>Two Wire Interface</td>
<td>Two Wire Interface Data</td>
</tr>
<tr>
<td>P59</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P60</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P61</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P62</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P63</td>
<td>Notch</td>
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</tr>
<tr>
<td>P64</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P65</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P66</td>
<td>Notch</td>
<td>No Connect</td>
</tr>
<tr>
<td>P67</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P68</td>
<td>Reserved</td>
<td>No Connect</td>
</tr>
<tr>
<td>P69</td>
<td>CONFIG_1</td>
<td>Ground</td>
</tr>
<tr>
<td>P70</td>
<td>+3.3 V</td>
<td>3.3 V Source</td>
</tr>
<tr>
<td>P71</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P72</td>
<td>+3.3 V</td>
<td>3.3 V Source</td>
</tr>
<tr>
<td>P73</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>P74</td>
<td>+3.3 V</td>
<td>3.3 V Source</td>
</tr>
<tr>
<td>P75</td>
<td>CONFIG_2</td>
<td>Ground</td>
</tr>
</tbody>
</table>
5 Supported Command and Feature Sets

The Intel SSD 540s Series supports all mandatory Advanced Technology Attachment (ATA) and Serial ATA (SATA) commands defined in the ACS-3 and SATA Revision 3.2 specifications. The mandatory and optional commands are defined in this section.

5.1 Supported ATA General Feature Command Set

Below are mandatory and optional ATA feature sets supported by Intel SSD 540s Series.

- 48-Bit Address
- General
- General Purpose Logging (GPL)
- Native Command Queuing (NCQ)
- Power Management
- Sanitize Device
- Security
- SMART
- Software Settings Preservation (SSP)

Below are mandatory and optional ATA commands supported by Intel SSD 540s Series.

Table 11: Supported ATA Commands and Feature Sets

<table>
<thead>
<tr>
<th>Commands</th>
<th>Feature Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLOCK ERASE EXT</td>
<td>Sanitize Device</td>
</tr>
<tr>
<td>CHECK POWER MODE</td>
<td>Power Management</td>
</tr>
<tr>
<td>CRYPTO SCRAMBLE EXT</td>
<td>Sanitize Device</td>
</tr>
<tr>
<td>DATA SET MANAGEMENT</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>DOWNLOAD MICROCODE</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>EXECUTE DEVICE DIAGNOSTIC</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>FLUSH CACHE</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>FLUSH CACHE EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>IDENTIFY DEVICE ¹</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>IDLE</td>
<td>Power Management</td>
</tr>
<tr>
<td>IDLE IMMEDIATE</td>
<td>Power Management</td>
</tr>
<tr>
<td>NOP</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ BUFFER</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ DMA</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ DMA EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>READ FPDMA QUEUED</td>
<td>Native Command Queuing</td>
</tr>
<tr>
<td>READ LOG DMA EXT</td>
<td>General Purpose Logging</td>
</tr>
<tr>
<td>READ LOG EXT</td>
<td>General Purpose Logging</td>
</tr>
<tr>
<td>Commands</td>
<td>Feature Set</td>
</tr>
<tr>
<td>--------------------------------</td>
<td>----------------------</td>
</tr>
<tr>
<td>READ MULTIPLE</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ MULTIPLE EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>READ NATIVE MAX ADDRESS</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>READ NATIVE MAX ADDRESS EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>READ SECTOR(S)</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ SECTOR(S) EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>READ VERIFY SECTOR(S)</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>READ VERIFY SECTOR(S) EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>SANITIZE FREEZE LOCK EXT</td>
<td>Sanitize Device</td>
</tr>
<tr>
<td>SANITIZE STATUS EXT</td>
<td>Sanitize Device</td>
</tr>
<tr>
<td>SECURITY DISABLE PASSWORD</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SECURITY ERASE PREPARE</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SECURITY ERASE UNIT</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SECURITY FREEZE LOCK</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SECURITY SET PASSWORD</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SECURITY UNLOCK</td>
<td>ATA Security</td>
</tr>
<tr>
<td>SEEK</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>SET FEATURES</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>SET MAX ADDRESS EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>SET MULTIPLE MODE</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>SLEEP</td>
<td>Power Management</td>
</tr>
<tr>
<td>SMART DISABLE OPERATIONS</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART ENABLE OPERATIONS</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART EXECUTE OFF-LINE IMMEDIATE</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART READ DATA</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART READ ATTRIBUTE THRESHOLDS</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART READ LOG</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART READ LOG SECTOR</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART RETURN STATUS</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART SAVE ATTRIBUTE VALUES</td>
<td>SMART</td>
</tr>
<tr>
<td>SMART WRITE LOG SECTOR</td>
<td>SMART</td>
</tr>
<tr>
<td>STANDBY</td>
<td>Power Management</td>
</tr>
<tr>
<td>STANDBY IMMEDIATE</td>
<td>Power Management</td>
</tr>
<tr>
<td>WRITE BUFFER</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>WRITE DMA</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>WRITE DMA EXT</td>
<td>48-Bit Address</td>
</tr>
</tbody>
</table>
## Commands

<table>
<thead>
<tr>
<th>Commands</th>
<th>Feature Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRITE DMA FUA EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>WRITE FPDMA QUEUED</td>
<td>Native Command Queuing</td>
</tr>
<tr>
<td>WRITE LOG DMA EXT</td>
<td>General Purpose Logging</td>
</tr>
<tr>
<td>WRITE LOG EXT</td>
<td>General Purpose Logging</td>
</tr>
<tr>
<td>WRITE MULTIPLE</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>WRITE MULTIPLE EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>WRITE MULTIPLE FUA EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>WRITE SECTOR(S)</td>
<td>ATA General Feature</td>
</tr>
<tr>
<td>WRITE SECTOR(S) EXT</td>
<td>48-Bit Address</td>
</tr>
<tr>
<td>WRITE UNCORRECTABLE EXT</td>
<td>ATA General Feature</td>
</tr>
</tbody>
</table>

### NOTES:

1. See the Appendix for details on the sector data returned after issuing an IDENTIFY DEVICE command.

### Security Features

#### 5.2 Sanitization Methods

Sanitization refers to a process that renders data inaccessible. Various sanitization methods are listed below.

##### 5.2.1 Secure Erase

Secure Erase runs the SECURITY ERASE UNIT command

<table>
<thead>
<tr>
<th>Table 12: Supported Secure Erase Modes and Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Secure Erase Mode</td>
</tr>
<tr>
<td>Normal Mode</td>
</tr>
<tr>
<td>Enhanced Mode</td>
</tr>
</tbody>
</table>

##### 5.2.1.2 Sanitize Device

<table>
<thead>
<tr>
<th>Table 13: Supported Sanitize Device Modes and Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
</tr>
<tr>
<td>Block Erase</td>
</tr>
<tr>
<td>Crypto Scramble Ext</td>
</tr>
</tbody>
</table>

### 5.3 DevSleep

Intel® SSD 540s Series supports the DevSleep feature. DevSleep must be enabled on the device by the host system through the SET FEATURES command. If DevSleep is enabled by the host, the host must drive the DevSleep signal to proper assert/de-assert voltage levels according to the SATA specification. Entry into DevSleep must be preceded by LPM slumber entry by host and device. The Intel SSD 540s Series also supports...
DevSleep_to_ReducedPwrState which allows the host to wake the drive using normal LPM COMWAKE out-of-band signaling.

For the Intel SSD 540s Series, the recommended total time to DevSleep for system active state is 6 sec. The AHCI* controller has 4 parameters used to define proper DevSleep operation between the host and drive. The following table provides those recommended values for the Intel SSD 540s Series.

### Table 14: DevSleep Control Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
<th>Control</th>
<th>Recommended Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>DITO</td>
<td>DevSleep Idle Time Out – number of milliseconds prior to host asserting DevSleep</td>
<td>Set by Host</td>
<td>Active (lid-up): 375</td>
</tr>
<tr>
<td>DM</td>
<td>DITO Multiplier – set once at boot-up</td>
<td>Set by Host</td>
<td>15</td>
</tr>
<tr>
<td>MDAT</td>
<td>Minimum DevSleep Assertion Time – minimum time in milliseconds for host to assert DevSleep</td>
<td>Reported by Drive</td>
<td>10</td>
</tr>
<tr>
<td>DETO</td>
<td>DevSleep Exit Time Out – max time in milliseconds from when DevSleep is negated to when device ready to detect OOB</td>
<td>Reported by Drive</td>
<td>20</td>
</tr>
</tbody>
</table>

**Total time to DevSleep entry = DITO * (DM+1)**

### 5.4 SMART Attributes

The following two tables list the SMART attributes supported by the Intel SSD 540s Series, and the corresponding status flags and threshold settings.

### Table 15: SMART Attributes

<table>
<thead>
<tr>
<th>ID</th>
<th>Attribute</th>
<th>Status Flags</th>
<th>Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>05h</td>
<td>Re-allocated Sector Count</td>
<td>SP:1 EC:1 ER:0 PE:0 OC:1 PW:0</td>
<td>0 (none)</td>
</tr>
<tr>
<td></td>
<td>The raw value of this attribute shows the number of retired blocks since leaving the factory (grown defect count).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>09h</td>
<td>Power-On Hours Count</td>
<td>SP:1 EC:1 ER:0 PE:1 OC:0 PW:0</td>
<td>0 (none)</td>
</tr>
<tr>
<td></td>
<td>The raw value reports the cumulative number of power-on hours over the life of the device, The On/Off status of the Device Initiated Power Management (DIPM) and Devsleep features will affect the number of hours reported. If DIPM and/or Devsleep are turned On, the recorded value for power-on hours does not include the time that the device is in those states.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0Ch</td>
<td>Power Cycle Count</td>
<td>SP:1 EC:1 ER:0 PE:1 OC:1 PW:10</td>
<td>0 (none)</td>
</tr>
<tr>
<td></td>
<td>The raw value of this attribute reports the cumulative number of power cycle events over the life of the device.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AAh</td>
<td>Available Reserved Space (See E8 Attribute)</td>
<td>SP:1 EC:1 ER:0 PE:1 OC:1 PW:10</td>
<td></td>
</tr>
</tbody>
</table>
### ID | Attribute | Status Flags | Threshold |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ABh</td>
<td>Program Fail Count</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>ACb</td>
<td>Erase Fail Count</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>AEh</td>
<td>Unexpected Power Loss</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>B7h</td>
<td>SATA Downshift Count</td>
<td>1 1 0 0 1 0</td>
<td>0</td>
</tr>
<tr>
<td>B8h</td>
<td>End-to-End Error Detection Count</td>
<td>1 1 0 0 1 1</td>
<td>90</td>
</tr>
<tr>
<td>BBh</td>
<td>Uncorrectable Error Count</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>BEh</td>
<td>Temperature</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>C0h</td>
<td>Power-Off Retract Count (Unsafe Shutdown Count)</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>C7h</td>
<td>CRC Error Count</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>E1h</td>
<td>Host Writes</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
<tr>
<td>E2h</td>
<td>Timed Workload Media Wear</td>
<td>1 1 0 0 1 0</td>
<td>0 (none)</td>
</tr>
</tbody>
</table>
### Table 16: SMART Attribute Status Flags

<table>
<thead>
<tr>
<th>Status Flag</th>
<th>Description</th>
<th>Value = 0</th>
<th>Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP</td>
<td>Self-preserving attribute</td>
<td>Not a self-preserving attribute</td>
<td>Self-preserving attribute</td>
</tr>
<tr>
<td>EC</td>
<td>Event count attribute</td>
<td>Not an event count attribute</td>
<td>Event count attribute</td>
</tr>
<tr>
<td>ER</td>
<td>Error rate attribute</td>
<td>Not an error rate attribute</td>
<td>Error rate attribute</td>
</tr>
<tr>
<td>PE</td>
<td>Performance attribute</td>
<td>Not a performance attribute</td>
<td>Performance attribute</td>
</tr>
<tr>
<td>OC</td>
<td>Online collection attribute</td>
<td>Collected only during offline activity</td>
<td>Collected during both offline and online activity</td>
</tr>
<tr>
<td>PW</td>
<td>Pre-fail warranty attribute</td>
<td>Advisory</td>
<td>Pre-fail</td>
</tr>
</tbody>
</table>
### 6 Certifications and Declarations

The following table describes the Device Certifications supported by the Intel SSD 540s Series.

**Table 17: Device Certifications and Declarations**

<table>
<thead>
<tr>
<th>Certification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RCM* Compliant</td>
<td>Compliance with the Australia/New Zealand Standard AS/NZS3548 and Electromagnetic Compatibility (EMC) Framework requirements of the Australian Communication Authority (ACA).</td>
</tr>
<tr>
<td>BSMI* Compliant</td>
<td>Compliance to the Taiwan EMC standard CNS 13438: Information technology equipment - Radio disturbance Characteristics - limits and methods of measurement, as amended on June 1, 2006, is harmonized with CISPR 22: 2005.04.</td>
</tr>
<tr>
<td>KCC*</td>
<td>Compliance with paragraph 1 of Article 11 of the Electromagnetic Compatibility Control Regulation and meets the Electromagnetic Compatibility (EMC) Framework requirements of the Radio Research Laboratory (RRL) Ministry of Information and Communication Republic of Korea.</td>
</tr>
<tr>
<td>Microsoft* WHCK/WHLK</td>
<td>Microsoft Windows Hardware Certification</td>
</tr>
<tr>
<td>RoHS* Compliant</td>
<td>Restriction of Hazardous Substance Directive</td>
</tr>
<tr>
<td>VCCI*</td>
<td>Voluntary Control Council for Interface to cope with disturbance problems caused by personal computers or facsimile.</td>
</tr>
<tr>
<td>SATA-IO*</td>
<td>Indicates certified logo program from Serial ATA International Organization.</td>
</tr>
<tr>
<td>Low Halogen</td>
<td>Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components on the finished assembly meet JS-709 requirements, and the PCB/substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environment.</td>
</tr>
</tbody>
</table>
## 7 Appendix

### 7.1 Identify Device

The following table describes the sector data returned from an identify device command.

**Table 18: Identify Device Returned Sector Data**

<table>
<thead>
<tr>
<th>Word</th>
<th>F = Fixed</th>
<th>V = Variable</th>
<th>X = Both</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>F</td>
<td></td>
<td></td>
<td>0040h</td>
<td>General configuration bit-significant information</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td>3FFFh</td>
<td>Obsolete - Number of logical cylinders (16,383)</td>
</tr>
<tr>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
<td>C837h</td>
<td>Specific configuration</td>
</tr>
<tr>
<td>3</td>
<td>X</td>
<td></td>
<td></td>
<td>0010h</td>
<td>Obsolete - Number of logical heads (16)</td>
</tr>
<tr>
<td>4-5</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Retired</td>
</tr>
<tr>
<td>6</td>
<td>X</td>
<td></td>
<td></td>
<td>003Fh</td>
<td>Obsolete - Number of logical sectors per logical track (63)</td>
</tr>
<tr>
<td>7-8</td>
<td>V</td>
<td></td>
<td></td>
<td>0h</td>
<td>Reserved for assignment by the CompactFlash® Association (CFA)</td>
</tr>
<tr>
<td>9</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Retired</td>
</tr>
<tr>
<td>10-19</td>
<td>F</td>
<td></td>
<td></td>
<td>varies</td>
<td>Serial number (20 ASCII characters)</td>
</tr>
<tr>
<td>20-21</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Retired</td>
</tr>
<tr>
<td>22</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Obsolete</td>
</tr>
<tr>
<td>23-26</td>
<td>F</td>
<td></td>
<td></td>
<td>varies</td>
<td>Firmware revision (8 ASCII characters)</td>
</tr>
<tr>
<td>27-46</td>
<td>F</td>
<td></td>
<td></td>
<td>varies</td>
<td>Model number (Intel® Solid State Drive)</td>
</tr>
<tr>
<td>47</td>
<td>F</td>
<td></td>
<td></td>
<td>8010h</td>
<td>7.0—Maximum number of sectors transferred per interrupt on multiple commands</td>
</tr>
<tr>
<td>48</td>
<td>F</td>
<td></td>
<td></td>
<td>4000h</td>
<td>Reserved</td>
</tr>
<tr>
<td>49</td>
<td>F</td>
<td></td>
<td></td>
<td>2F00h</td>
<td>Capabilities</td>
</tr>
<tr>
<td>50</td>
<td>F</td>
<td></td>
<td></td>
<td>4000h</td>
<td>Capabilities</td>
</tr>
<tr>
<td>51-52</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Obsolete</td>
</tr>
<tr>
<td>53</td>
<td>F</td>
<td></td>
<td></td>
<td>0007h</td>
<td>Words 88 and 70:64 valid</td>
</tr>
<tr>
<td>54</td>
<td>X</td>
<td></td>
<td></td>
<td>3FFFh</td>
<td>Obsolete - Number of logical cylinders (16,383)</td>
</tr>
<tr>
<td>55</td>
<td>X</td>
<td></td>
<td></td>
<td>0010h</td>
<td>Obsolete - Number of logical heads (16)</td>
</tr>
<tr>
<td>56</td>
<td>X</td>
<td></td>
<td></td>
<td>003Fh</td>
<td>Obsolete - Number of logical sectors per logical track (63)</td>
</tr>
<tr>
<td>57-58</td>
<td>X</td>
<td></td>
<td></td>
<td>00FBFC10h</td>
<td>Obsolete</td>
</tr>
<tr>
<td>59</td>
<td>V</td>
<td></td>
<td></td>
<td>B110h</td>
<td>Sanitize/Multiple Sector settings</td>
</tr>
<tr>
<td>60-61</td>
<td>F</td>
<td></td>
<td></td>
<td>varies</td>
<td>Total number of user-addressable sectors</td>
</tr>
<tr>
<td>62</td>
<td>X</td>
<td></td>
<td></td>
<td>0h</td>
<td>Obsolete</td>
</tr>
<tr>
<td>63</td>
<td>F</td>
<td></td>
<td></td>
<td>0007h</td>
<td>Multi-word DMA modes supported/selected</td>
</tr>
<tr>
<td>Word</td>
<td>F = Fixed V = Variable X = Both</td>
<td>Default Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>---------------------------------</td>
<td>---------------</td>
<td>-------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>F</td>
<td>0003h</td>
<td>PIO modes supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>F</td>
<td>0078h</td>
<td>Minimum multiword DMA transfer cycle time per word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>66</td>
<td>F</td>
<td>0078h</td>
<td>Manufacturer's recommended multiword DMA transfer cycle time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>67</td>
<td>F</td>
<td>0078h</td>
<td>Minimum PIO transfer cycle time without flow control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>F</td>
<td>0078h</td>
<td>Minimum PIO transfer cycle time with IORDY flow control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>69</td>
<td>F</td>
<td>4D10h</td>
<td>Additional Supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>F</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>71-74</td>
<td>F</td>
<td>0h</td>
<td>Reserved for IDENTIFY PACKET DEVICE command</td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>F</td>
<td>001Fh</td>
<td>Queue depth</td>
<td></td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>F</td>
<td>070Eh</td>
<td>Serial ATA capabilities</td>
<td></td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>F</td>
<td>0086h</td>
<td>Reserved for future Serial ATA definition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>F</td>
<td>014Ch</td>
<td>Serial ATA features supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>V</td>
<td>0040h</td>
<td>Serial ATA features enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>F</td>
<td>07FCh</td>
<td>Major version number</td>
<td></td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>F</td>
<td>FFFFe</td>
<td>Minor version number</td>
<td></td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>F</td>
<td>7468h</td>
<td>Command set supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>F</td>
<td>7409h</td>
<td>Command sets supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>F</td>
<td>6163h</td>
<td>Command set/feature supported extension</td>
<td></td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>V</td>
<td>7469h</td>
<td>Command set/feature enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>86</td>
<td>V</td>
<td>B409h</td>
<td>Command set/feature enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>87</td>
<td>V</td>
<td>6163h</td>
<td>Command set/feature default</td>
<td></td>
<td></td>
</tr>
<tr>
<td>88</td>
<td>V</td>
<td>407Fh</td>
<td>Ultra DMA Modes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>89</td>
<td>F</td>
<td>0002h</td>
<td>Time required for security erase unit completion</td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>F</td>
<td>0001h</td>
<td>Time required for enhanced security erase completion</td>
<td></td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>V</td>
<td>00FEh</td>
<td>Current advanced power management value</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>V</td>
<td>FFFFe</td>
<td>Master Password Revision Code</td>
<td></td>
<td></td>
</tr>
<tr>
<td>93</td>
<td>F</td>
<td>0h</td>
<td>Hardware reset result: the contents of bits (12:0) of this word shall change only during the execution of a hardware reset</td>
<td></td>
<td></td>
</tr>
<tr>
<td>94</td>
<td>V</td>
<td>0h</td>
<td>Vendor’s recommended and actual acoustic management value</td>
<td></td>
<td></td>
</tr>
<tr>
<td>95</td>
<td>F</td>
<td>0h</td>
<td>Stream minimum request size</td>
<td></td>
<td></td>
</tr>
<tr>
<td>96</td>
<td>V</td>
<td>0h</td>
<td>Streaming transfer time - DMA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>97</td>
<td>V</td>
<td>0h</td>
<td>Streaming access latency - DMA and PIO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>98-99</td>
<td>F</td>
<td>0h</td>
<td>Streaming performance granularity</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100-103</td>
<td>V</td>
<td>varies</td>
<td>Maximum user LBA for 48-bit address feature set</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Word</td>
<td>F = Fixed</td>
<td>Default Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>-----------</td>
<td>---------------</td>
<td>-------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>104</td>
<td>V</td>
<td>0h</td>
<td>Streaming transfer time - PIO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>105</td>
<td>F</td>
<td>0008h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>106</td>
<td>F</td>
<td>4000h</td>
<td>Physical sector size / logical sector size</td>
<td></td>
<td></td>
</tr>
<tr>
<td>107</td>
<td>F</td>
<td>0h</td>
<td>Inter-seek delay for ISO-7779 acoustic testing in microseconds</td>
<td></td>
<td></td>
</tr>
<tr>
<td>108-111</td>
<td>F</td>
<td>varies</td>
<td>Unique ID</td>
<td></td>
<td></td>
</tr>
<tr>
<td>112-115</td>
<td>F</td>
<td>0h</td>
<td>Reserved for world wide name extension to 128 bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>116</td>
<td>V</td>
<td>0h</td>
<td>Reserved for technical report</td>
<td></td>
<td></td>
</tr>
<tr>
<td>117-118</td>
<td>F</td>
<td>0h</td>
<td>Words per logical sector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>119</td>
<td>F</td>
<td>401Ch</td>
<td>Supported settings</td>
<td></td>
<td></td>
</tr>
<tr>
<td>120</td>
<td>F</td>
<td>401Ch</td>
<td>Command set/feature enabled/supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td>121-126</td>
<td>F</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>127</td>
<td>F</td>
<td>0h</td>
<td>Removable Media Status Notification feature set support</td>
<td></td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>V</td>
<td>0021h</td>
<td>Security status</td>
<td></td>
<td></td>
</tr>
<tr>
<td>129-159</td>
<td>X</td>
<td>varies</td>
<td>Vendor-specific</td>
<td></td>
<td></td>
</tr>
<tr>
<td>160</td>
<td>F</td>
<td>0h</td>
<td>CompactFlash Association (CFA) power mode 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>161-167</td>
<td>X</td>
<td>0h</td>
<td>Reserved for assignment by the CFA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>168</td>
<td>F</td>
<td>0007h (M.2)</td>
<td>Nominal Form Factor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>169</td>
<td>X</td>
<td>0001h</td>
<td>Data set management Trim attribute support</td>
<td></td>
<td></td>
</tr>
<tr>
<td>170-173</td>
<td>F</td>
<td>0h</td>
<td>Additional Product Identifier</td>
<td></td>
<td></td>
</tr>
<tr>
<td>174-175</td>
<td>F</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>176-205</td>
<td>V</td>
<td>0h</td>
<td>Current media serial number</td>
<td></td>
<td></td>
</tr>
<tr>
<td>206</td>
<td>X</td>
<td>0039h</td>
<td>SCT Command Transport</td>
<td></td>
<td></td>
</tr>
<tr>
<td>207-208</td>
<td>X</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>209</td>
<td>X</td>
<td>4000h</td>
<td>Alignment of logical blocks within a physical block</td>
<td></td>
<td></td>
</tr>
<tr>
<td>210-211</td>
<td>X</td>
<td>0h</td>
<td>Write-Read-Verify Sector Count Mode 3 (DWord)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>212-213</td>
<td>X</td>
<td>0h</td>
<td>Write-Read-Verify Sector Count Mode 2 (DWord)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>214</td>
<td>X</td>
<td>0h</td>
<td>NV Cache Capabilities</td>
<td></td>
<td></td>
</tr>
<tr>
<td>215-216</td>
<td>X</td>
<td>0h</td>
<td>NV Cache Size in Logical Blocks (DWord)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>217</td>
<td>X</td>
<td>0001h</td>
<td>Nominal media rotation rate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>218</td>
<td>X</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>219</td>
<td>X</td>
<td>0h</td>
<td>NV Cache Options</td>
<td></td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>X</td>
<td>0h</td>
<td>Write-Read-Verify feature set</td>
<td></td>
<td></td>
</tr>
<tr>
<td>221</td>
<td>X</td>
<td>0h</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Default Value Table

<table>
<thead>
<tr>
<th>Word</th>
<th>F = Fixed</th>
<th>V = Variable</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>222</td>
<td>X</td>
<td></td>
<td>10FFh</td>
<td>Transport major version number</td>
</tr>
<tr>
<td>223</td>
<td>X</td>
<td></td>
<td>0h</td>
<td>Transport minor version number</td>
</tr>
<tr>
<td>224-229</td>
<td>X</td>
<td></td>
<td>0h</td>
<td>Reserved</td>
</tr>
<tr>
<td>230-233</td>
<td>X</td>
<td></td>
<td>0h</td>
<td>Extended Number of User Addressable Sectors (QWord)</td>
</tr>
<tr>
<td>234</td>
<td>X</td>
<td></td>
<td>0002h</td>
<td>Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h</td>
</tr>
<tr>
<td>235</td>
<td>X</td>
<td></td>
<td>0080h</td>
<td>Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h</td>
</tr>
<tr>
<td>236-254</td>
<td>X</td>
<td></td>
<td>0h</td>
<td>Reserved</td>
</tr>
<tr>
<td>255</td>
<td>X</td>
<td></td>
<td>varies</td>
<td>Integrity word</td>
</tr>
</tbody>
</table>

**NOTES:**

- **F = Fixed.** The content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
- **V = Variable.** The state of at least one bit in a word is variable and may change depending on the state of the device or the commands executed by the device.
- **X = F or V.** The content of the word may be fixed or variable.

### 7.2 Models

The following table lists the available M.2 single-sided models of the Intel® SSD 540s Series.

**Table 19: Available Models**

<table>
<thead>
<tr>
<th>Model String</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSDSCCKW120H6</td>
<td>120GB</td>
</tr>
<tr>
<td>SSDSCCKW180H6</td>
<td>180GB</td>
</tr>
<tr>
<td>SSDSCCKW240H6</td>
<td>240GB</td>
</tr>
<tr>
<td>SSDSCCKW360H6</td>
<td>360GB</td>
</tr>
<tr>
<td>SSDSCCKW480H6</td>
<td>480GB</td>
</tr>
<tr>
<td>SSDSCCKW010X6</td>
<td>1000GB</td>
</tr>
</tbody>
</table>