White Paper

Improving Pin-to-Pin Timing in Stratix & Stratix GX Devices

Introduction

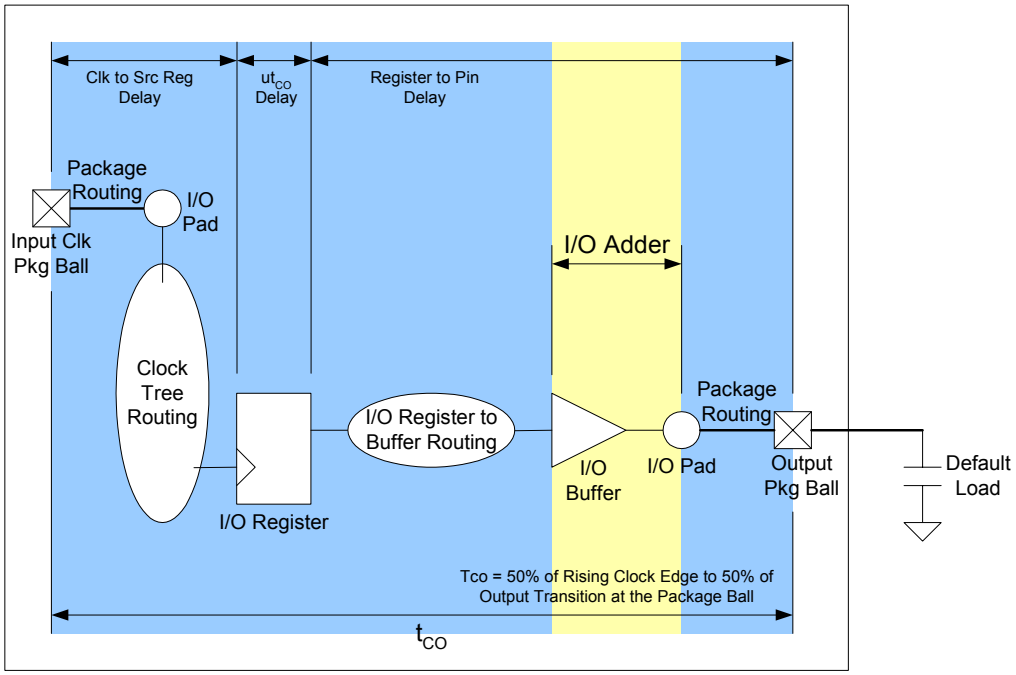
Meeting the I/O timing requirements for complex systems can be a challenging task in FPGA designs. The programmability of FPGAs offers various options to improve pin-to-pin timing in designs. This paper discusses techniques that can be used to improve the t_{CO} and t_{PD} output timing for Stratix™ and Stratix™ GX devices with a focus on t_{CO}.

What is t_{CO}?

t_{CO} is defined as the maximum time required to obtain a valid output at an output pin that is fed by a register after a clock signal transition on an input pin that clocks the register. This time always represents an external pin-to-pin delay. In Quartus® II, it is reported as the 50% of the rising clock input edge to 50% of the output transition at the respective package pins. t_{CO} is calculated using the following equation:

$\mathbf{t_{CO}}$ = *<clock to source register delay>* + *<micro clock to output delay>* + *<register to pin delay>*

Figure 1. t_{CO} Components



The t_{PD} can be defined as the delay from the source of the combinational logic to the output pin. The components of the t_{PD} include the routing delay from the source of the combinational logic plus the delay through the output buffer and the package routing to the pin.

Phase Shifting of Clock Using the PLL

By utilizing the phase-locked loop (PLL) to feed the registers in the data path, the t_{CO} timing is improved. Since the PLL compensates for the clock delay to the register, the clock routing component of the t_{CO} is reduced, and result in a faster t_{CO} overall.

Additionally, PLLs can be used to phase shift the clock in the negative direction, to further improve the t_{CO} timing. By phase shifting the clock that feeds the registers in the data path, the relationship between the data output transition and the input clock can be varied. Depending on degree of the phase shift, it may be possible to achieve a very small t_{CO} value. Fast Input Register and Fast Output Register Logic Options should be turned on to utilize the register in the I/O Element to ensure the fastest register to output pin timing.

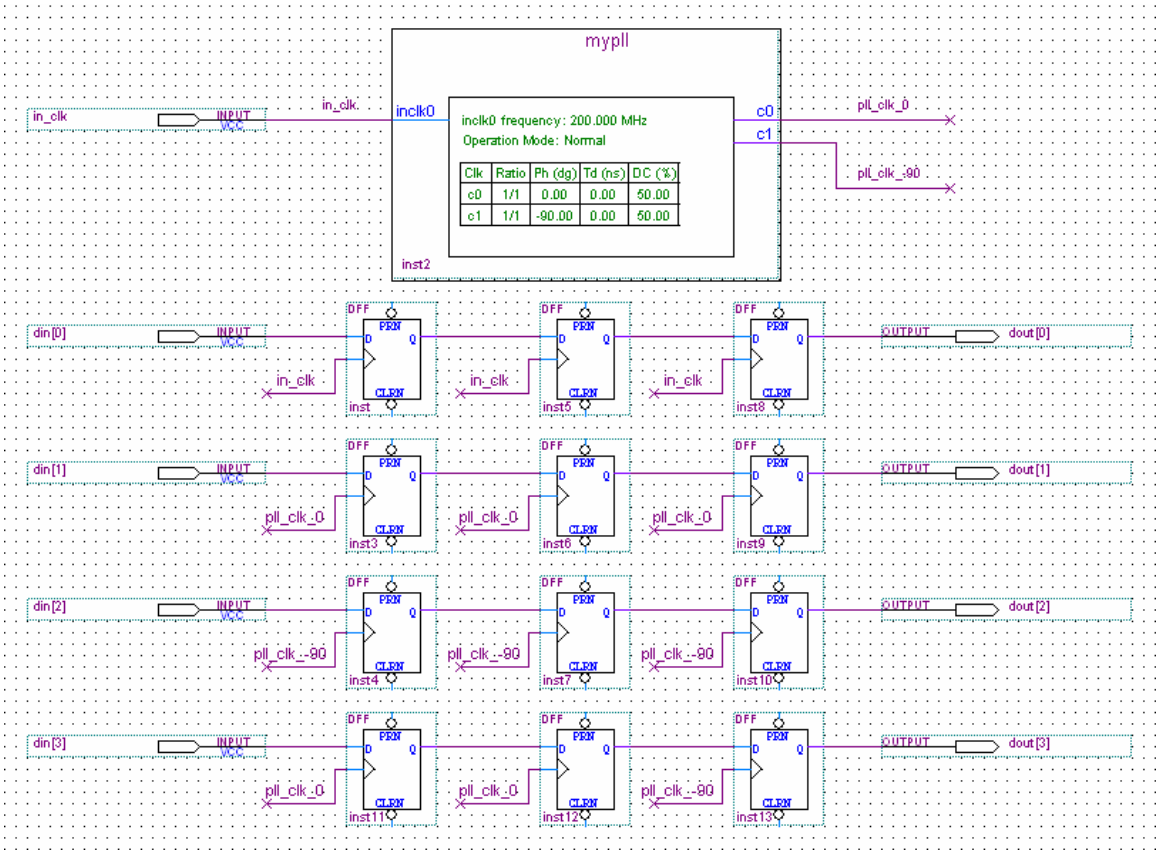
The drawback of phase shifting is that the t_{SU} timing will be inversely affected. The timing improvements gained for t_{CO} result in timing degradations for t_{SU}. It is possible to achieve a fast t_{SU} and t_{CO}, if multiple clock domains are used in the same data path. For example, if the input clock is used to feed the input register and the PLL output clock with a phase shift is used to feed the output register, it is possible to achieve timing improvements for both t_{SU} and t_{CO}. The multiple clock domain approach requires much more stringent register-to-register timing. Additionally, the Min t_{CO} needs to be considered, as a fast t_{CO} will make it more difficult to meet t_{HOLD} requirements of the downstream device. The trade-offs to each approach need to be carefully considered before selecting the best method for improving pin-to-pin timing.

Figure 2 illustrates the various setups used for the timing analsis shown in table 1.

Table 1. Timing Analysis

Pin	t_{CO} (ns)	t_{SU} (ns)	Description
dout[0]/din[0]	5.663	1.692	No PLL
dout[1]/din[1]	2.746	1.208	PLL with 0 deg phase shift
dout[2]/din[2]	1.499	2.411	PLL with -90 deg phase shift
dout[3]/din[3]	1.143	1.408	PLL with multi-clock domain

Figure 2. Sample t_{CO} Design



The PLL phase shifting technique will help improve t_{CO} but will not affect the t_{PD} as there is no clock network in the t_{PD} path. One approach to help improve the t_{PD} is to move the combinational logic close to the output pin to help reduce the routing delays.

Increasing the Current Drive Strength Setting

Another technique to improve the pin-to-pin timing is to increase the Current Drive Strength Setting. By changing the drive strength setting, the properties of the output buffer are changed, and the I/O Adder portion of the t_{CO} improves. Depending on the load present at the output pin, increasing the drive strength offers significant timing improvements. A larger drive strength increase results in a larger t_{CO} and t_{PD} improvement.

Table 2 illustrates the timing improvement by increasing the drive strength for a 3.3V LVTTL standard with a 10pF load.

Table 2. I/O Adder for 3.3V LVTTL with 4mA Base

Drive Strength Setting	t_{CO} & t_{PD} Change (ps)
4mA	0
8mA	-328
12mA	-819
16mA	-834
24mA	-1325

When utilizing this technique, the Simultaneous Switching Noise (SSN) considerations should be taken into account. As you increase the drive strength, the SSN restrictions become more stringent, as the faster edge rates combined with the number of Simultaneous Switching Outputs may cause ground and power bounce. Carefully weigh the system noise and power considerations when utilizing this method.

Utilizing the Fast Slew Rate Option

The fast slew rate option is another technique where the output buffer properties are altered to improve the t_{CO} and t_{PD} timing. Similar to the current drive strength method, the I/O adder portion of the t_{CO} path is improved, resulting in faster pin-to-pin timing. It should be noted that the Fast Slew Rate option is the default in Quartus II and this technique can only be used if the slow slew rate option was selected in the design.

The same SSN considerations must be considered when utilizing the fast slew rate method.

Conclusion

Stratix & Stratix GX devices offer flexible solutions to improve the pin-to-pin timing of the device. Techniques such as PLL phase shifting, increasing current drive strength, and utilizing fast slew rate options, give designers choices to help meet the timing requirements of their systems. The advantages and trade-offs should be carefully weighed to select the best option for their systems.

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