An Analytical Review of FPGA Logic Efficiency in Stratix, Virtex-II & Virtex-II Pro Devices

Introduction

This white paper will demonstrate through concrete benchmark data and architectural comparisons that Altera's Stratix™ FPGA products have a 9% logic resource utilization advantage over Xilinx Virtex-II Pro FPGA products. Since the Virtex-II Pro and Virtex-II families have similar FPGA architectures, the Stratix family's logic efficiency advantage over Virtex-II Pro can also be applied to Virtex-II. Therefore, the benchmark data and analysis for Virtex-II are not provided here.

Comparison Methodology

Each FPGA architecture has unique features that differentiate it from other FPGAs. Furthermore, FPGA vendors use different terminologies in their literature and CAD tools to describe the logic capacity of their products. These differences have made comparing logic efficiency between FPGAs a difficult task.

Nevertheless, each of the advanced FPGA architectures is constructed from a sea of basic logic units, where each unit consists of a four-input look-up table (LUT), programmable register, and any associated specialized circuits, such as a carry chain, cascade logic, primitive logic gates and mutiplexers. Even when a FPGA contains additional dedicated circuits such as multipliers, the bulk of a typical design's logic functions are still implemented by these basic units. Therefore, this generic basic unit can be used to fairly measure the size of a design across different FPGA architectures.

Altera uses the "Logic Element" (LE) methodology to measure the logic capacity of a FPGA. Each LE consists of a four-input LUT, a programmable register and associated specialized circuits, and it satisfies the definition of the aforementioned basic logic unit. An LE is a measurable unit in both the Stratix and Virtex-II Pro families. Thus, the unit of an LE will be used throughout this paper as the metric to compare the logic utilization efficiency between the Stratix and Virtex-II Pro families. With the generalized LE definition, a Stratix logic array block (LAB) has 10 LEs, a Virtex-II Pro slice has 2 LEs and a Virtex-II Pro configurable logic block (CLB) has 8 LEs.

The benchmark comparison is conducted using 97 real customer designs with design sizes up to 61,000 LEs. The design size categorization is based on the logic utilization reported after place-and-route when a design is compiled targeting the Stratix and Virtex-II Pro FPGA families. Synplify 7.1A was used as the logic synthesis tool for both the Stratix and Virtex-II Pro FPGA families. The Quartus® II software version 2.2 and ISE 5.1i service pack 2 were used to place-and-route the designs in the Stratix and Virtex-II Pro FPGA families, respectively. Default settings were used for Synplify, the Quartus II software, and ISE. Through our extensive experiments, we found that on average default settings deliver the best results in terms of both logic usage and performance.

Table 1 describes the device families, synthesis, and place-and-route tools used in the benchmark activities.

Table 1. Benchmark Setup

Vendor	Device Family	Synthesis Tool	Place-and-Route Tool
Altera	Stratix FPGA Family	Synplify 7.1A	Quartus II version 2.2
Xilinx	Virtex-II Pro FPGA Family	Synplify 7.1A	ISE 5.1i Service Pack 2

The extracted logic resource utilization data is based on the results reported by the Quartus II software and ISE after place-and-route. An LE is considered used whenever one or more of its composing parts — LUT, register and any associated specialized circuitry — are used.

Synthesis Tools Resource Utilization Reporting

When a design is successfully synthesized, synthesis tools often report an estimation for the logic and resources used by the design. However, the logic utilization reported by the synthesis tool should only be treated as a rough estimate because of advanced fitting algorithms, such as register packing, and other factors such as black-boxing, megafunctions, and Quartus II netlist optimization techniques. True logic utilization should be obtained from place-and-route tool’s compilation reports. [Refer to Altera® Tech Brief, TB 84: “*Differences in Logic Utilization between Quartus II & Synplify Report Files*”]

Benchmark Data and Scatter Plot

Of the 97 benchmarked designs, 80% (78 designs) are more logic efficient when the design is implemented in a Stratix FPGA than in a Virtex-II Pro FPGA. On average, a design targeting Stratix uses 9% fewer LEs than the same design targeting Virtex-II Pro devices. Figure 1 shows the results of the entire benchmark design set where each data point represents the logic utilization ratio, **r**, for a given design. The ratio, r, is calculated via Equation 1.

Equation 1.

$$\mathbf{r} = \frac{\textbf{(Stratix LE Usage)}}{\textbf{(Virtex-II Pro LE Usage)}}\Bigg|_{\textit{a given design}}$$

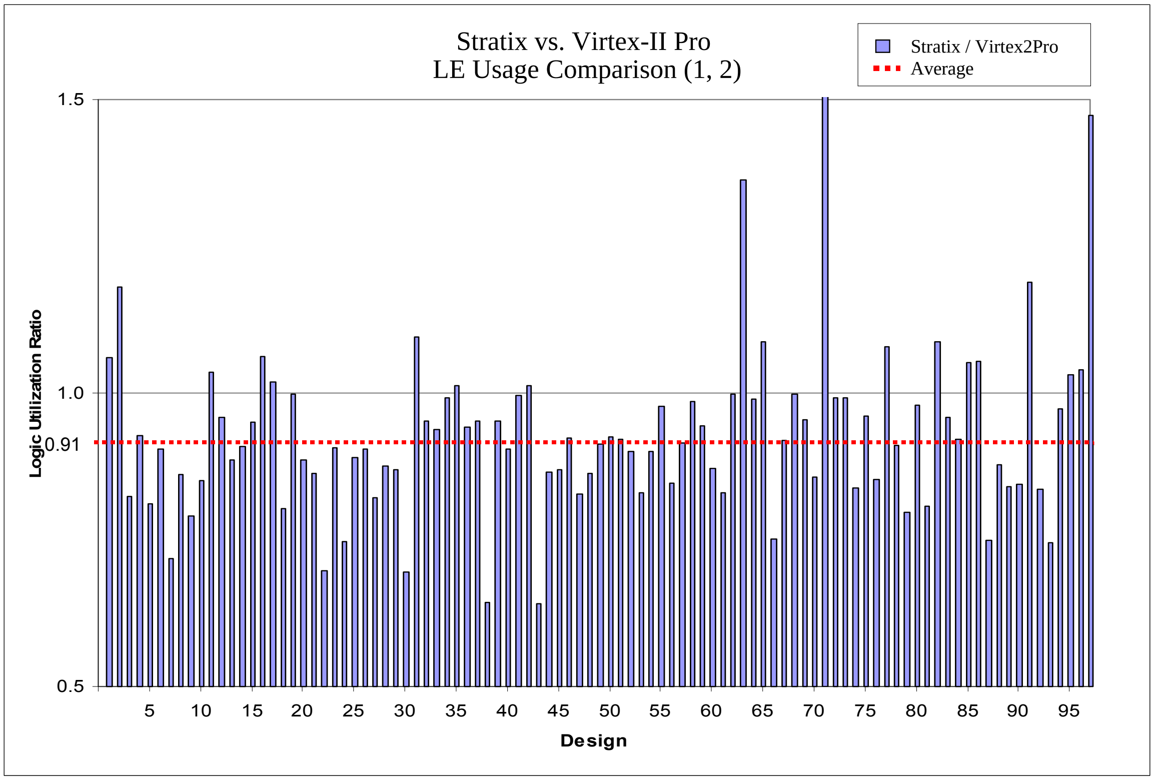
When **r** = 1, a design is using the same amount of logic resources (LEs) in both Stratix and Virtex-II Pro devices. When **r** < 1, a design is using fewer LEs in Stratix devices when compared to the same design implemented in Virtex-II Pro. When **r** > 1, such design is using fewer LEs in Virtex-II Pro than in Stratix devices.

The average of the samples is calculated via Equation 2.

Equation 2.

$$\textbf{Average} = \textbf{Geometric Mean}\left[\frac{\textbf{(Stratix LE Usage)}}{\textbf{(Virtex-II Pro LE Usage)}}\Bigg|_{\textit{design set}}\right]$$

Figure 1. Stratix vs. Virtex-II Pro Device LE Usage Comparison



Note to Figure 1:

(1) Data points are sorted in the ascending order of density with the smallest design on the left side of the graph and the largest design on the right side of the graph.

(2) The logic utilization of a design depends on the design details, optimization techniques, CAD software algorithms and device capabilities. The benchmark data shows typical results. Individual result may vary with designs.

Out of the benchmark design suite, 41% of the designs implemented in the Stratix architecture are at least 10% more efficient than the same design implemented in Virtex-II Pro. Eleven percent of the designs are at least 20% more efficient in Stratix FPGAs. The high logic efficiency achieved by the Stratix architecture is due to the combination of the LE and LAB structures, embedded DSP blocks, flexible memory structure, the Quartus II software's register packing algorithm, and other dedicated features.

Table 2 summarizes the designs by the LE resources required by Stratix and Virtex-II Pro devices to implement these 97 designs.

Table 2. Stratix vs. Virtex-II Pro Design LE Usage Summary

LE Utilization Ratio (Stratix/Virtex-II Pro)	**> 1**	**1-0.9**	**0.9-0.8**	**0.8-0.7**	**< 0.7**
Design Count (97 Total)	19	38	29	7	4
% of design out of all 97 designs	20%	39%	30%	7%	4%

DSP Blocks Advantage

Stratix FPGAs offer up to 28 powerful DSP blocks that are capable of performing pipelined multiply-and-accumulate (MAC) functions at up to 278 MHz while significantly reducing the amount of logic needed for a DSP-intensive design. The DSP blocks are not just simple multipliers; each DSP block contains several configurable dedicated multiplier blocks and adder/output blocks to combine five arithmetic operations — multiplication, addition, subtraction, accumulation, and summation — to meet the requirements of complex functions and to provide improved performance. No extra programmable logic resources are required when these arithmetic functions are implemented in the DSP blocks. Figure 2 shows the block diagram for a DSP block.

Figure 2. DSP Block Diagram

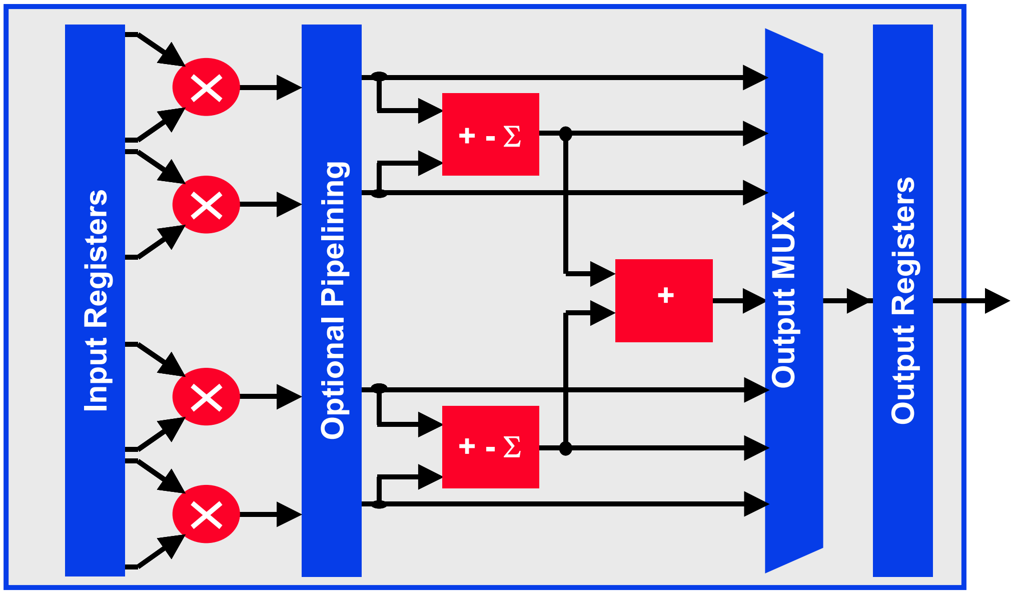


Table 3 details different DSP block operation modes.

Table 3. DSP Block Operation Modes (1)

DSP Block Mode	Description
Simple Multiplier	Eight 9-bit by 9-bit or four 18-bit by 18-bit independent multipliers or one 36-bit by 36-bit multiplier.
Multiply-accumulator	Two 18-bit multiply-accumulators. Each MAC output can be up to 52 bits wide for a maximum 36-bit result with 16-bit accumulation.
Two-multiplier Adder	Output two sums or differences for up to 18-bit multiplicands, or 4 sums or differences for 9-bit or smaller multiplicands. Example applications: complex multiplication, FFT functions and complex FIR filters.
Four-multiplier Adder	The DSP block adds the results of two adders/subtractors/accumulators in the final stage (summation block). Example applications: 1-dimensional and 2-dimensional filters.

Note to Table 3:

(1) Refer to Altera Application Note, AN 214:Using the DSP Blocks in Stratix and Stratix GX Devices.

With this flexibility, the Stratix DSP block can be configured to efficiently fit a design's requirement. The DSP block also contains embedded input, output, pipeline, and scan chain registers that further reduce the programmable logic needed in the FPGA logic.

Table 4 summarizes the logic and dedicated resource requirements for implementing arithmetic operations in Stratix and Virtex-II Pro FPGAs.

Table 4. Stratix vs. Virtex-II Pro Multiplier Implementation Resource Requirement Comparison

Multiplier Size	Resources			
	Stratix		Virtex-II Pro	
	DSP Block	LE (2)	18x18 Multiplier Block	LE (2)
Signed 9x9	1/8 *(1)*	0 [0]	1	0 [36]
Signed 18x18	1/4 *(1)*	0 [0]	1	0 [72]
Signed 36x36	1	0 [0]	4	326 [397]
18x18 MAC	1/2	0 [0]	1	49 [134]
18x18 Complex Multiplication	1	0 [0]	4	76 [153]
4 Tap, 16-bit FIR Filters with Parallel Inputs	1	[0]	4	[280]
4 Tap, 16-bit FIR Filters with Serial Inputs	1	[0]	4	[199]

Notes to Table 4:

(1) One DSP block can be configured as 8 independent 9x9 multipliers or 4 independent 18x18 multipliers.

(2) The numeric value in brackets [] indicates the number of LEs needed when both input and output signals are registered.

In the benchmark suite, Stratix FPGAs consume fewer logic resources than the Virtex-II Pro family in 11 of the 16 designs that contain DSP blocks. On average, the Stratix family shows a 3% logic utilization advantage over the Virtex-II Pro family in these 16 designs.

Memory Advantage

The Stratix FPGA family's advanced TriMatrix™ memory architecture offers 3 different sizes of embedded memory — M512, M4K, and M-RAM (576 bits, 4608 bits and 589824 bits respectively) — that are tailored to suit different memory requirements in different designs. In the Virtex-II Pro architecture, a memory can be realized only through the use of distributed SelectRAM+ or the 18Kb block SelectRAM+. When a memory is implemented in the distributed SelectRAM+, LUTs are configured as both memories and address decoding logic. These LUTs can no longer be used to construct logic functions in a design and thus the logic capacity of the FPGA is reduced.

Table 5 contains the comparisons of how various sized memories can be implemented in the Stratix and Virtex-II Pro architectures.

Table 5. Stratix and Virtex-II Pro Memory Resources Usage Comparison

Memory Size	Stratix Memory Resources	Virtex-II Pro Memory Resources
< 1K bits	One or two M512s	LEs used as distributed SelectRAM+
		One 18Kb block SelectRAM+ (94+% unused)
1K bits - 10K bits	Multiple M512s or M4Ks	LEs used as distributed SelectRAM+
		One 18Kb block SelectRAM+ (44-94% unused)
>= 10 Kbits	M4Ks or M-RAM	1 or Multiple 18Kb block SelectRAM+

For example, to implement a 2K-bit dual-port RAM using distributed SelectRAM+ consumes 459 LEs. If an 18Kb block SelectRAM+ is used to implement this RAM, only 11% of this block SelectRAM+ is utilized. The remaining 89% will be left unused and cannot be used for other purposes. The Stratix family can efficiently implement this RAM in four M512 memory blocks and each block is 100% utilized.

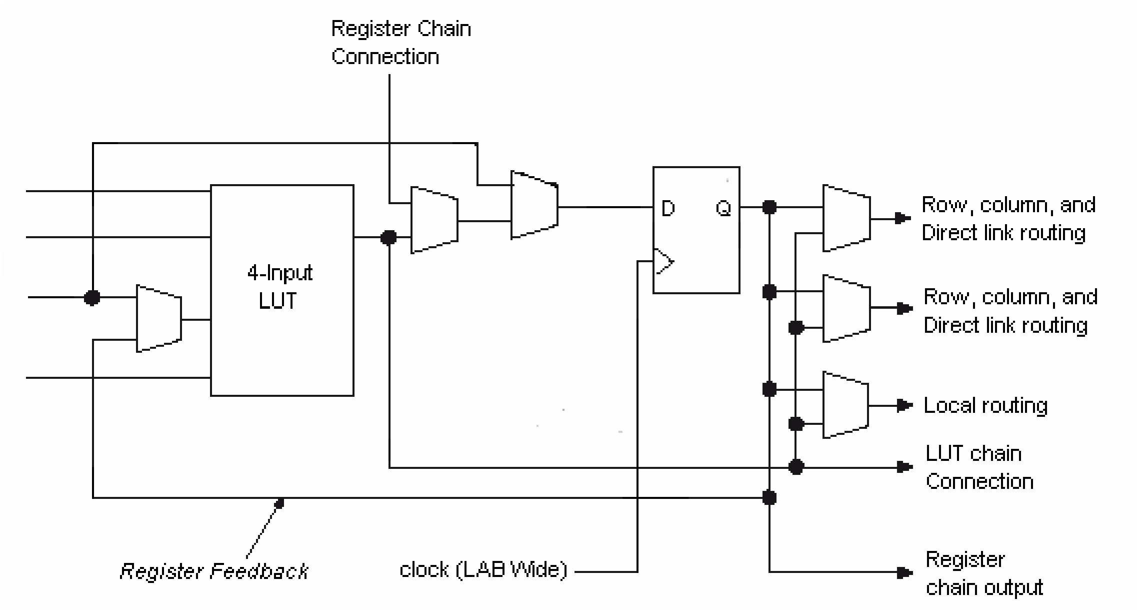
The benchmark shows that 19 designs contain distributed SelectRAM+ when they are implemented in Virtex-II Pro FPGAs. When these designs are re-targeted to the Stratix architecture, the memory requirements are satisfied by the combination of M512 and M4K memory blocks. The Stratix family uses fewer logic resources in 16 of these 19 designs. On average, the Stratix family shows a 10% logic utilization advantage over the Virtex-II Pro family in these 19 designs.

Register Packing Advantage

The efficiency of a design's logic utilization depends on many different factors — the FPGA architecture, the synthesis tool, the place-and-route tool, and the coding of the design itself. The Stratix architecture was designed to be highly routable by allowing every LE in the device to use both its LUT and register for independent functions and still route successfully. The Quartus II software fully leverages this architectural advantage and aggressively makes an LE perform "double-duty" by packing a LUT and register into a single LE.

Figure 3 shows the extra register-to-LUT (register feedback) and register-to-register (register chain) connectivity in the Stratix architecture that Virtex-II Pro lacks. These extra dedicated connections are very fast in order to enhance the circuit speed. They are also useful for avoiding routing congestion when both a LUT and register are packed in the same LE.

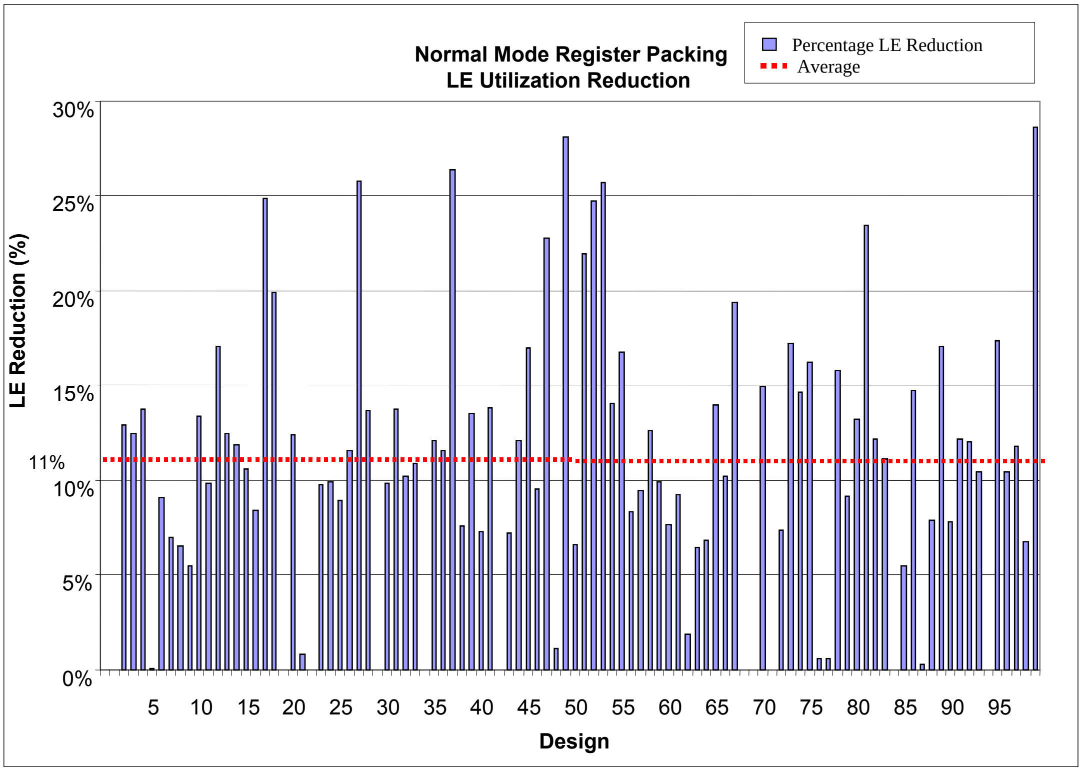
Figure 3. Register Feedback and Register Chain Structure in an LE



In addition to the advanced architecture Stratix FPGAs offer, Altera's Quartus II software is equipped with a powerful feature, called register packing. Register packing actively takes the registers in a design and packs them into unrelated LEs that only use the LUTs. This process reduces the size of a design and often fits a design into a smaller device. Register packing is set to operate in Normal mode by default.

Our research (Figure 4) has shown that, on average, register packing in Normal mode can improve the logic utilization efficiency by 11% without any performance degradation. On average, the LE usage can be further reduced by another 9% with a 5% reduction in f_{max} if "Minimize Area with Chains" mode is used. The benchmark data presented in this paper are using Normal mode register packing.

Figure 4. Normal Mode Register Packing Logic Utilization Improvement (1)



Notes to Figure 4:

(1) The data points are extracted from post place-and-route results reported by Quartus II v.2.2

Shift Registers Advantage

Shift registers can be efficiently implemented in the Stratix family by either the embedded memory blocks or the enhanced LE structure. Deep and wide shift registers can be implemented in the dedicated M512 or M4K memory blocks. Smaller shift registers can be implemented in the enhanced LE structure, known as the LE register chain.

The Stratix family has up to 1118 M512 and 520 M4K blocks and they can be configured to implement shift registers with various depth, width and taps. A M512 block can offer up to 576 bits with maximum width of 18 bits. For example, an 18-bit wide, 32-bit deep shift register needs one M512 block and 12 LEs, but requires 39 LEs in the Virtex-II Pro architecture. [Refer to Altera Application Note, AN 203: *"Using TriMatrix Embedded Memory Blocks in Stratix Devices."*]

Table 6 shows examples of deep and wide shift register implementations in the Stratix and Virtex-II Pro families.

Table 6. Deep & Wide Shift Register Comparison between Stratix & Virtex-II Pro Families

Shift Register Size	Configuration	Stratix	Virtex-II Pro
576 bits	18-bit wide and 32-bit deep	1 M512 + 12 LEs	39 LEs
4096 bits	32-bit wide and 128-bit deep	1 M4K + 16 LEs	261 LEs

The register chain is a feature that uses special routing resources to chain registers in LEs together to act as a shift register. The register used in the register chain is independent of the 4-input LUT in the same LE. Since a designer can implement shift registers by "recycling" the unused registers in the LEs whose LUTs are already configured to perform other logic functions, the use of the register chain is at no cost and can assist in reducing the total logic usage of a design. Figure 3 shows the register chain structure in an LE.

LVDS Dedicated SERDES Advantage

The Stratix FPGA family provides dedicated serializer-deserializer (SERDES) for the low voltage differential signaling (LVDS) interface. The dedicated SERDES can improve the required timing for the high-speed interfaces, simplify the design process, and alleviate the need to consume FPGA logic resources for data serialization and de-serialization.

A 4-channel (1channel = a transmitter and receiver pair) LVDS design [refer to Xilinx Application Note, XAPP265: "High-Speed Data Serialization and Deserialization (840 Mb/s LVDS)"] consumes 180 LEs when it is implemented in the Virtex-II Pro architecture. However, a similar design can be implemented in the Stratix family without consuming any FPGA logic resources. Take the Stratix EP1S80 device as another example. When 136 dedicated high-speed LVDS channels (1channel = a transmitter and receiver pair) are used, no programmable logic resources will be consumed. To implement the same number of LVDS channels in a Virtex-II Pro device requires 6120 LEs.

Conclusion

The Stratix architecture includes advanced features such as the highly routable LE and LAB structures, DSP blocks, TriMatrix memory, register chain, and dedicated LVDS SERDES that contribute significantly in reducing the logic resources requirements of a design. Also, the Quartus II software register packing feature further strengthens this logic utilization advantage. Our benchmark data has shown that on average, a design targeting Stratix FPGAs uses 9% fewer logic resources than the same design targeting Virtex-II Pro. It has been demonstrated through empirical benchmark data and architecture analysis that the Stratix FPGA family is more efficient in logic utilization compared to Virtex-II Pro.

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