
Building Flexible, Cost-Efficient Broadband Access Equipment Line Cards

Telecommunications equipment manufacturers (TEMs) are facing tough challenges with triple play (voice, video and data offerings) concentration and distribution equipment, including digital subscriber line access multiplexers (DSLAMs), optical line terminals (OLTs), and multiservice access nodes (MSANs). While there are multiple media options that deliver different services, each media requires a different type of networking component to handle the required access protocols, traffic engineering, and throughput.

The dedicated engineering resources needed to support each media type results in huge expenses associated with each line termination card including ADSL, VDSL, EPON, and GPON. These types of equipment line cards must be designed with significantly more bandwidth to support non-blocking Internet protocol television (IPTV), additional protocol handling, traffic management delivering high quality of service (QoS), particularly to voice and video traffic, and more stringent multicast performance supporting current IPTV requirements and future Internet appliances, including gaming and video/voice conferencing.

Another major challenge is the ability to offer everything for less. Increasing international competition has put tremendous pricing pressure on DSLAM providers. The dollar per port price TEMs pay for DSLAMs has fallen precipitously in recent years. The only way to maintain margin is to lower the cost of building DSLAM hardware.

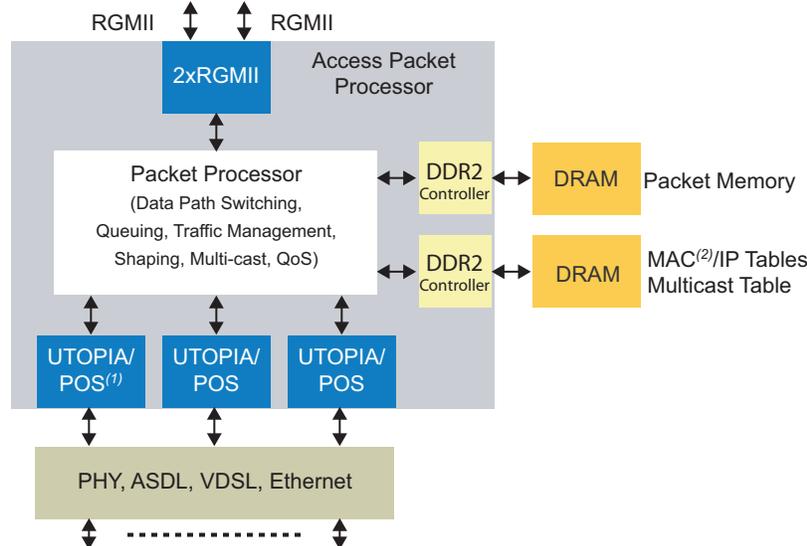
A third challenge faced by TEMs is creating platforms to host their own unique features and functionality while differentiating their solution. One way to differentiate is to build a platform-based solution that will enable them to adapt and handle new networking or protocol requirements without having to purchase them from the silicon vendor that may then sell the same solution to competitors.

In this paper, we will examine the access packet processor (APP) requirements of DSLAM line cards, including those needed to address the challenges discussed above. A brief discussion will follow on the semiconductor industry trends, the architectural features of Ethernity Networks' commercially available FPGA access flow processor (AFP), the ENET3000, plus the characteristics of the ENET3000 and why it is the ideal choice for line termination cards.

Next-Generation Access Aggregation Line Card Processing Requirements

The ideal APP needs throughput, flexibility, scalability, and low power to address these challenges and to meet the demands of next-generation DSLAMs. See [Figure 1](#).

Figure 1. Access Packet Processor Block Diagram



Throughput

It is critical that an APP have the necessary throughput to enable non-blocking performance to all media and ports connected on specific line termination module, as well as the capability to deliver new revenue-generating services and enforce the QoS contracted with all customers. Throughput should be deterministic and not vary based on the type of network traffic internal processing functionality. The APP must allow bandwidth to be flexibly partitioned based on port, service, and direction, while having a low power requirement and low line-card cost.

As the video services portion of the triple play is deployed, the need for throughput and APP performance in the DSLAM line card increases by an order of magnitude (up to 30 Mbps per port). Not only must each port provide more throughput, but the nature of triple-play services is to duplicate the video stream on a line card for the required ports that register to specific service. No longer can DSL aggregation bandwidth be so largely oversubscribed. The demands of video streams are too large and too constant to allow the level of oversubscription tolerated in pure data services DSL deployments. The throughput of an APP lacking deterministic performance must be measured based on its worst-case performance to ensure committed service rates are not impacted when handling “tortuous” protocols.

A 72-port ADSL2+ line card might need to handle over 2.5 Gbps of throughput only for video. This assumes three unique high-definition (HD) broadcast or video-on-demand channels per port at 6 Mbps per HD video stream. A 32-port VDSL line card offering 100M/100M service per port would require 5.0 Gbps. In another example, a remote DSLAM supporting 48 ports requires an additional gigabit throughput to support several DSLAMs connected into a single ring.

Flexibility

The ideal APP has the exact interface and packet processing capabilities needed for the line card it is designed for. Since access equipment vendors have a family of line cards for their platforms, the ideal APP must be available as either a family of devices or as a device with flexible interfaces. If the APP has too many interfaces trying to meet all requirements, the line-card design will be burdened with additional board area, cost, and power to support unneeded functionality. Worse, if the APP does not support the necessary interfaces to meet these requirements, either it cannot be used or will require additional external devices or logic to compensate for this shortcoming.

An ideal APP should also have the capabilities to support a full range of protocols—including PPPoA, IPoA, PPPoEoA, EoA, Tagged Ethernet, SNAP, Q-in-Q, MAC-in-MAC, and MPLS—as well as the flexibility to easily handle future, as yet undefined protocols.

Scalability

While sufficient throughput is needed for high-speed and high port count line cards, a solution that scales down in price (including external memory), power, and board area is needed for other line cards. System vendors gain product lifecycle efficiencies by using the same technology, components, and suppliers across a wide range of products, so APPs must be scalable and flexible enough to be added to products with a wide range of performance and applications. System vendors are looking for a generic interworking and traffic manager solution that is scalable from ADSL through VDSL, as well as Ethernet and PONs that increase original equipment manufacturer (OEM) scalability and help reduce carrier capital expenses (CAPEX) while improving operating expenditures (OPEX).

Low Power

An APP and the associated memory must remain within the power budget of the system. Some designs operate without external power, and total system power is restricted to that available from the twisted pairs. Line cards designed for existing platforms face a firm budget set when the DSLAM platform was first developed. If an APP is significantly below this power budget, the system can benefit from higher reliability and potentially greater flexibility in the number and type of cards that can be supported by the platform (the platform's maximum configuration). Line cards designed for new systems also face stringent power budgets. A low-power APP provides several potential benefits, including lower system cost, greater system reliability, and greater port densities.

Enabling Universal Line Termination Processing

The ENET3000 features a unique architecture that supports using low-cost FPGAs with a combination of DDR2 memory to provide advanced functionality and flexibility, while competing with packet processors and network processors that typically offer better functionality, performance, and cost. The ENET Family is implemented in the Altera® Cyclone® II EP2C70 FPGA, supporting up to 5 Gbps, and in Stratix® II FPGAs (EP2S90 and EP2S130) for 20-Gbps support.

Ethernity's ENET3000 leverages a paradigm shift in ASIC development that enables complex and high-volume designs to be cost-effectively manufactured with FPGAs. The associated large increases in mask and development costs have left only the highest volume applications able to afford the investment required to move a design into the leading-edge processes (90 nm today and 65 nm coming soon). Altera's Cyclone II and Stratix II families are implemented with a 90-nm process and offer the logic density, speed, power, and cost advantages associated with these leading-edge process technologies.

Combining an Ethernity ENET3000 AFP with an Altera Cyclone II FPGA provides a highly efficient architecture for low-cost, high-density FPGAs. The ENET3000 handles classification, framing, packet editing, forwarding, and all traffic management in pipelined micro-engines. Considering the amount of logic required the ENET3000 architecture is highly efficient. Twenty-five percent of the gates are needed relative to what is found in a typical RISC-based network APP. This gate- or logic-efficient architecture can be implemented in an Altera Cyclone II FPGA for a low-cost 1- to 5-Gbps FPGA AFP solution or in a Stratix II FPGA for a high-performance solution supporting 5 to 20 Gbps.

Providing reconfigurable modularity to an APP architecture redefines broadband access line card design and deployment flexibility, scalability, and cost savings. The AFP provides multiple line interface types and reprogrammable interworking options on a single, modular architecture. Interchangeable line interface units offer a cost-effective way of adding service interface types and customized line cards that precisely match port count and packet processing line card demands. This capability allows designers to use the exact line interface needed, per port, instead of having to build separate line cards. Reconfigurable, build-as-you-need-it deployments substantially reduce capital costs. Adding incremental bandwidth accommodates unpredictable growth and changing traffic patterns, as well as eliminates costly unused ports.

In fixed line card architecture, the need for different port counts and service types forces TEMs to develop multiple line card designs based on different packet processors that increases the initial costs and creates bandwidth-specific

solutions. Inflexibility also increases total cost of ownership as the number of development teams multiply, and limits cross-platform scalability.

In contrast, addressing multiple service types and port counts with a single reconfigurable access packet processor architecture substantially lowers overall system cost and provides a scalable bandwidth independent solution. Flexible line interface options and protocol interworking functions enhance network performance, evolution, and multiple-service convergence while reducing operational complexity and expenses. The unique capabilities of an AFP enable flexible access line card design and simplify scalability for future growth.

Table 1 shows the development cost associated with the design of multiple line cards based on fixed access line card architecture. This assumes a non-blocking solution that operates at line speed for all ports, hence each solution is based on a different network or packet processor.

Table 1. Development Resource for Multiple Line Cards—Based on Fixed Architecture

	8-16 DSL Ports IP DSLAM	48 - 96 Ports ADSL IP DSLAM	24 - 48 Ports VDSL	10 GbE Ports	4 - 8 Ports of PONs	Total Dev. Engineers
Software Engineers	4	4	4	-	6	18
Board Engineers	3	4	4	1	4	15
Component Solution	Low-end processor	3-Gbps network processor	6-Gbps network processor	20-Gbps network processor	20-Gbps network processor	

Table 2 shows the same development cost based on universal line termination architecture. Comparing Tables 1 and 2 shows that using a universal line termination processor with reconfigurable interfaces dramatically reduces the overall development cost of a DSLAM design.

Table 2. Development Resource for Multiple Line Cards—Based on Universal Line Termination Architecture

	8-16 DSL or 6 FE/ Ports	48 - 96 Ports ADSL	24 - 48 Ports VDSL	10 GbE Ports	4 - 8 Ports of PONs	Total Dev. Engineers
Software Engineers	4	Same software platform	Same software platform	Same software platform	Same software platform	4
Board Engineers	2	2	1	1	2	8
Component Solution	Altera HC210 at below \$20	Altera Cyclone II EP2C70	Altera Cyclone II EP2C70	Altera Stratix	Altera Stratix	

TEMs can realize a 70% reduction in development costs as well as an equal amount to OPEX and CAPEX amounts when a single manufacturing and procurement platform is used for all line termination modules.

ENET3000 FPGA Access Flow Processor Addresses TEM Line Card Requirements

Ethernity Networks' ENET3000 AFP offers 5-Gbps deterministic performance, low power, and the capability to handle today's network traffic, while providing the flexibility to easily adapt to new network protocols and traffic management needs. The ENET3000 is based on several micro engines providing an intuitive programming model for supporting new protocols, flexible classification, and forwarding through the programmability of 32 search tables that

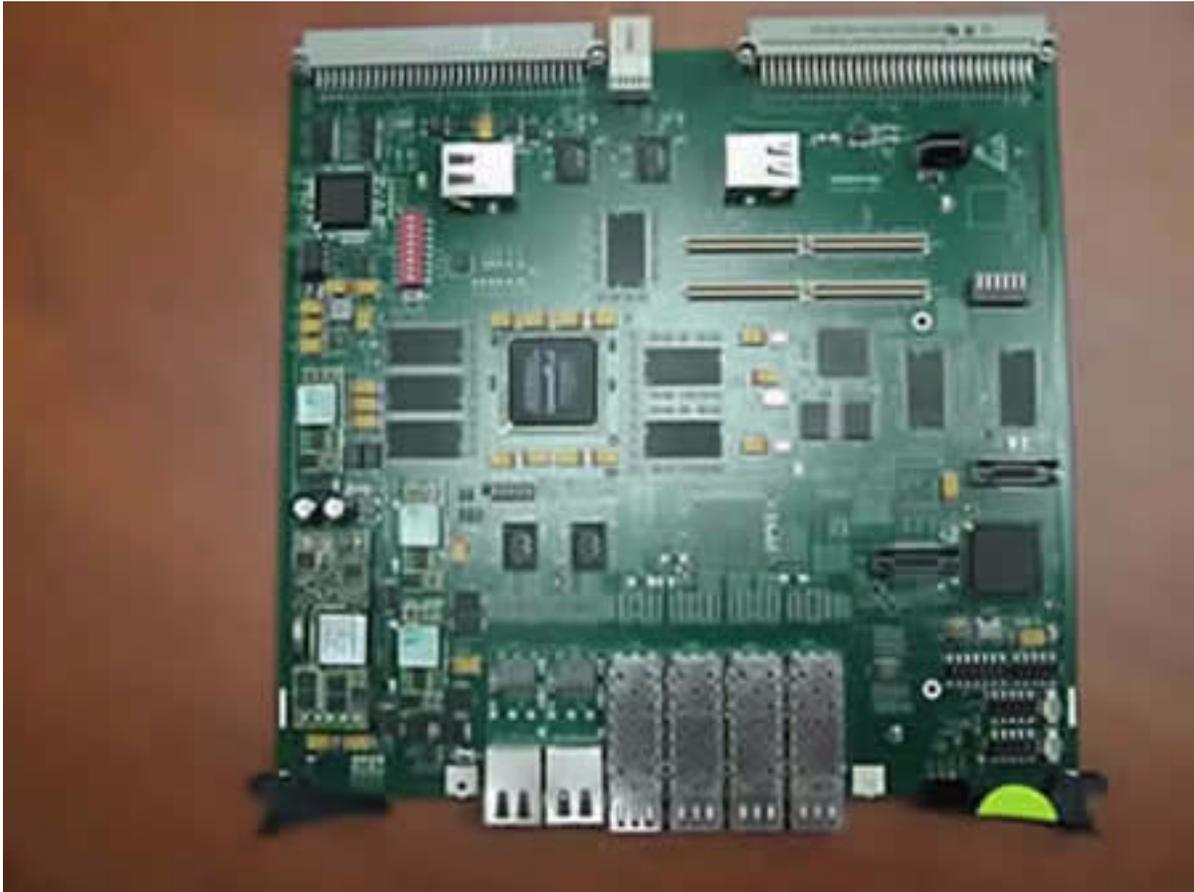
search up to 128,000 entries, programmable packet editing, and advanced traffic management. By offering the ENET3000 AFP solution in an FPGA, the access equipment designer receives a number of advantages associated with FPGA design, including customization of interfaces, ability to upgrade in the field, ability to incorporate other board logic, and rapid development and prototyping. These capabilities differentiate the ENET3000 from standard network processors, while offering important advantages to access equipment design.

Performance

The ENET3000 architecture is comprised of a staged pipeline. The tasks of parsing, classification, forwarding, traffic management, SAR, policing, and packet editing are each handled by one or more engines in the pipeline. The data pipeline width is 64 bits and the engine runs at 78 MHz, so a worst-case packet size of 64 bytes results in a throughput of 7.5 millions of packets per second (Mpps) or 5 Gbps.

Implemented in a Cyclone II FPGA, the ENET3000's 5-Gbps network traffic performance is well beyond the capabilities of most network processors available for access applications, such as DSLAM line cards. Network processors capable of this throughput are too expensive and consume too much power to be acceptable for typical DSLAM line-card deployments. See [Figure 2](#).

Figure 2. Cyclone II Access Packet Processor Reference Design



Flexibility

Implementing an AFP in an FPGA has many advantages, particularly the flexibility achieved on several levels. At any time, the many configuration registers and tables of the ENET3000 can be pre-configured or altered to handle a very intuitive programming model based on a simple API with a very large range of network traffic types and traffic

management/QOS requirements. The Ethernity FPGA solution offers the flexibility to customize interfaces, so the designer is not limited by the interfaces offered by an ASSP vendor. GMII, Utopia, SPI, POS, and unique customer-defined interfaces can be combined to suit the needs of the application. Additionally, the Ethernity FPGA solution offers the flexibility to upgrade a product in the field. While products are often deployed with no definitive plans to upgrade or alter installed units, the option of being able to alter the hardware in the FPGA offers important insurance against unforeseen events. This capability is important to many carriers who prefer to future-proof their systems with the option of field upgradeability.

Scalability

The ENET Family can be scaled from 2 Gbps to 20 Gbps by selecting the FPGA (Altera Cyclone II EP2C505 or EP2C70, or Stratix II EP2S90) and the number of external memory interfaces. See [Table 3](#).

Table 3. Examples of DSLAM Line Card Configurations

Line Card Type	Product	Interfaces		Simplex Bandwidth		DDR Memory
		Ethernet	Other	BPS	PPS	
2 x 10GbE	ENET4000	2 x SPI-4	Option for 20 x GbEs	20G		8
48-port VDSL2	ENET3500	4xPOS		5G	7M	6
32-port VDSL2	ENET3400	3xPOS		4G	5.5M	6
72-port ADSL2+	ENET3250A	2xRGMII	Utopia2 Master 3 D/S & 1 U/S	2.5G	3.5M	4
24-port ADSL2+	ENET3100A	2xSMII	Utopia2 Master	>1G	1.2M	3

Low Cost and Low Power

Ethernity delivers its 2- and 5-Gbps solutions on low-cost Altera Cyclone II FPGAs and its 20-Gbps solution on Altera's Stratix II FPGAs. APPs developed on state-of-the-art 90-nm FPGAs have several time-to-market and cost-saving benefits, including design automation, flexibility, and reduced development risk. Ethernity Networks has taken advantage of these benefits to accelerate AFP development in the dynamic IP-DSLAM market and adapt to constantly evolving standards.

Ethernity also leverages the design flexibility afforded by Altera's Stratix II FPGA-to-structured ASIC migration solution to easily create customized designs according to individual customer specifications. The ENET family supports line cards for multiservice platforms including 96-port dual latency nonblocking ADSL2+, nonblocking 32-port 100/100 VDSL2, multiport Fast Ethernet, Gigabit Ethernet, and Fiber-to-the-Home (FTTH).

A secondary benefit of the ENET3000's cost-efficient architecture is low power consumption. When processing a given amount of network traffic, the ENET3000's optimized architecture uses much less logic and less switching relative to a RISC processor—even when the processor's instruction set is tailored for networking applications. The ENET3000 requires well under 4 watts of power while handling 5 Gbps of network traffic.

The Ethernity FPGA solution offers the capability of adding logic to an FPGA that allows incorporation of miscellaneous board functions onto the FPGA. Many access cards designed with RISC NPUs also require FPGAs to implement features not supported by the NPU (such as framing or channel bonding) and to implement miscellaneous board logic. Ethernity's AFP is an access card's only FPGA. Unused logic on the ENET3000 is available to implement various types of board logic such as GPIO, timers, or other customer-specific functions.

Conclusion

There are numerous requirements for line termination access packet processors that must be met to fulfill the design challenges for DSLAM, OLT, and MSAN broadband access line cards. An FPGA-based access flow processor such as the ENET3000 combines the reconfigurability, performance, and scalability of FPGA and structured ASIC technologies with the best aspects of a customized, access packet processor architecture on a single chip. This combination provides the scalability, flexibility, and low-cost that designers need to deliver a wide range of programmable access packet processor solutions offering optimized product differentiation, customized packet processing, and rapid time-to-market.



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