SOLUTION BRIEF

Intel® FPGA Programmable Acceleration Card Solutions for Financial Services Industry (FSI)

2D PDE Solver Accelerator for Financial Applications

About the Solution

This reference design is an Intel® FPGA targeted OpenCL™ implementation of a 2D parabolic partial differential equation (PDE) solver based on a modified Craig-Sneyd Alternate Direction Implicit (ADI) scheme intended for acceleration of financial applications such as option pricing.

The accelerator is a numerical solver for 2D parabolic partial differential equation, a type of PDE commonly found in financial applications where the equation to be solved has the general form of:

$$\frac{\partial V}{\partial t} = a\frac{\partial^2 V}{\partial x^2} + b\frac{\partial V}{\partial x} + c\frac{\partial^2 V}{\partial y^2} + d\frac{\partial V}{\partial y} + e\frac{\partial^2 V}{\partial x \partial y} - rV$$

where coefficient **r** is a function of **t**, and coefficients **a**, **b**, **c**, **d**, and **e** can be dependent on x, y, and t. To reduce the amount of data required to express and store coefficients a, b, c, d, and e, instead of allowing them to be arbitrary functions (of x, y, and t), they are required to be separable and take the following form:

$$\omega = \omega_t(t) + \omega_x(x,t).\omega_x(y,t)$$

For the current implementation, the x and y dimensions are discretized into a finite difference grid of fixed size ***NX . NY***, where ***NX*** is 100 and ***NY*** is 50. The t dimension is discretized into a maximum of 103 steps. Variable step sizes are supported across all dimensions.

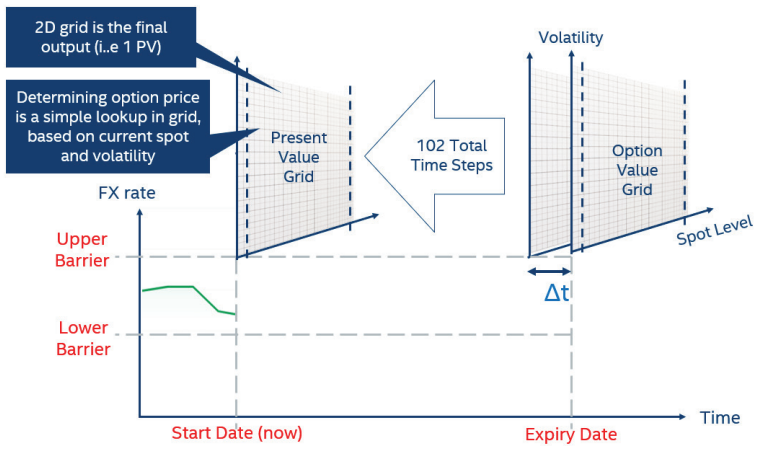

Figure 1. Illustration of the 102 step PDE Solver for FX Rate

Authors

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Built to Scale with Intel FPGA Financial Libraries

Intel will be delivering over 250 library functions in 2019 enabling you to develop your own financial algorithms targeted for your implementation. This library includes a vast array of functions including statistics, linear algebra, and math primitives. To enable easy development of your algorithms with the financial library functions we have built a platform with a full software stack to enable you to accelerate and orchestrate on FPGAs through OpenCL™. The PDE solver reference design leverages the orchestration capabilities of the software stack to deploy the PDE solver on four Intel Arria® 10 FPGA programmable acceleration cards on a single server.

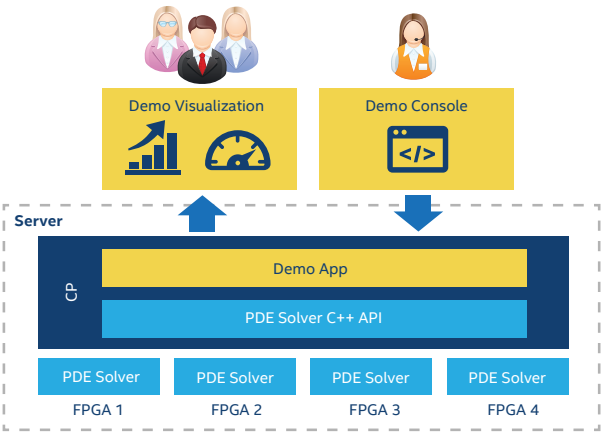

Figure 2. Data Center Orchestration Flow of Acceleration Platform

Figure 3. Actual Image of the Server Setup

Delivering Performance

Figure 4 shows the type of performance you should expect to get with our mid-range Intel Arria 10 FPGAs. There is an estimated 4X performance improvement expected going to our high-end Intel Stratix® 10 FPGAs†. Along with that, with the ability to orchestrate between multiple FPGAs the performance results show a linear improvement in performance as you scale. With this performance, the CPU utilization required the use of only one core, leaving the rest of the cores free to perform additional computations.

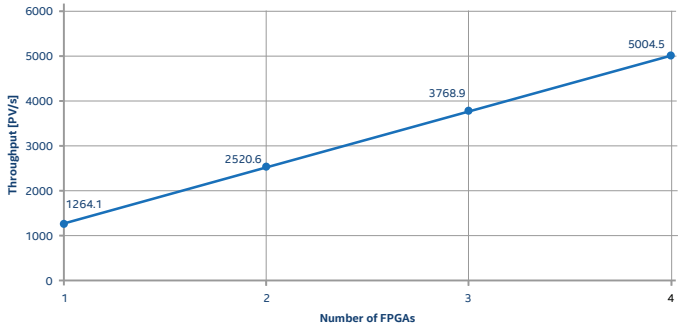

Figure 4. Linear Scalability for PDE Solver

Learn More

To learn more and get additional details on our libraries and reference designs, contact your local sales representative.

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

For more information go to www.intel.com/benchmarks.

Performance results are based on testing as of 29th March 2019 and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.

§ Configurations: The configuration is tested using a server with four Intel Arria10 Programmable Acceleration Cards, tested on 29th March 2019 by Intel.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. Check with your system manufacturer or retailer or learn more at intel.com.