

Stratix V Hard IP for PCI Express IP Core Release Notes

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If a release note is not available for a specific IP core version, the IP core has no changes in that version.

Stratix V Hard IP for PCI Express IP Core v16.1

Table 1: v16.1 October 2016

Description	Impact
For the Avalon-MM with DMA interface, increased the maximum DMA transfer size to 1 megabyte (MB) for both the 128- and 256-bit interfaces.	Reduces the number of descriptors required to transfer data.

Related Information

- [Stratix V Avalon-ST Interface for PCIe Solutions User Guide](#)
For the Avalon-ST Interface to the Application Layer.
- [V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide](#)
For the Avalon-MM interface and DMA functionality.
- [Stratix V Avalon-MM Interface for PCIe Solutions User Guide](#)
For the Avalon-MM interface with no DMA.
- [Stratix V Avalon-ST Interface with SR-IOV PCIe Solutions User Guide](#)
For the Avalon-ST interface with Single Root I/O Virtualization (SR-IOV)
- [Errata for the Stratix V Hard IP for PCI Express IP Core in the Knowledge Base](#)
- [Introduction to FPGA IP Cores](#)
Provides general information about all FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- [Creating Version-Independent IP and Qsys Simulation Scripts](#)
Create simulation scripts that do not require manual updates for software or IP version upgrades.
- [Project Management Best Practices](#)
Guidelines for efficient management and portability of your project and IP files.

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Stratix V Hard IP for PCI Express IP Core v16.0

Table 2: v16.0 May 2016

Description	Impact
For the V-Series Avalon [®] Memory-Mapped (Avalon-MM) DMA for PCI Express IP Core, rearchitected the Write DMA module for the 128-bit interface to the Application Layer.	Provides higher throughput for external memories.
For the V-Series Avalon-MM DMA for PCI Express IP Core, the 256-bit interface to the Application Layer now supports a maximum transfer size of 64 kilobytes (KB).	Large transfers require fewer descriptor table entries.
For the Avalon Streaming (Avalon-ST) with Single Root I/O Virtualization (SR-IOV) variant, removed support for the 128-bit interface to the Application Layer.	Beginning in Quartus [®] Prime 16.0, Altera recommends the 256-bit interface to the Application Layer for all new designs. If you have a mature design using the 128-bit interface, continue to use the 15.1 release. For designs in the early stages of development, Altera recommends that you move to the 16.0 software and the 256-bit interface.
For the Avalon-ST with SR-IOV variant, changed address map for the following registers: <ul style="list-style-type: none"> SR-IOV Virtualization Extended Capabilities ARI Secondary PCI Express Extended Capability Header 	If you update to the Quartus Prime 16.0 software, you must update your hardware and software to use the new register addresses.

Stratix V Hard IP for PCI Express IP Core v15.0

Table 3: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if Enable burst capability for RXM BAR2 port is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.

Description	Impact
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Stratix V Hard IP for PCI Express IP Core v14.1

Table 4: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Stratix V Hard IP for PCI Express IP Core v14.0

Table 5: v14.0 June 2014

Description	Impact
Added preliminary support for Stratix V Hard IP for PCI Express with SR-IOV (Single Root I/O Virtualization).	-
<p>Made the following changes for the V-Series PCIe with Avalon-MM DMA Interface (previously called the Avalon-MM 256-bit Hard IP for PCI Express IP Core).</p> <ul style="list-style-type: none"> Revised programming model and optimized the performance of the Descriptor Controller. Added support for either 128- or 256-bit interface to the Application Layer. Added support for 64-bit addressing, making address translation unnecessary. Added support for optional bursting RX Master for BAR2. Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM for Gen3 variants. Due to the many changes, the support level has reverted to preliminary. 	The Descriptor Controller IP core included in the 14.0 release is significantly different from the one included in 13.1. Altera recommends that you update to v14.0. Altera no longer support v13.1.

Description	Impact
<p>Made the following changes to the Avalon-MM Stratix V Hard IP for PCI Express IP core:</p> <ul style="list-style-type: none"> • Added access to selected Configuration Space registers and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals. • Added support for 64-bit addressing, making address translation unnecessary. • Added parameters to enable 256 completion tags with completion tag checking performed in Application Layer. • Simulation support for Phase 2 and Phase 3 equalization when requested by third-party BFM. • Increased CRA address to 14 bits from 12 bits. 	<p>All of these new features are optional. If you include an optional feature that changes the port signature of your IP core, you must regenerate your design and connect the signals</p>
<p>Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i>.</p>	-

Stratix V Hard IP for PCI Express IP Core v13.1

Table 6: v13.1 November 2013

Description	Impact
<p>Support for a Avalon-MM 256-Bit Hard IP for PCI Express Gen3 x8 with DMA is final.</p>	-
<p>Support for Gen2 CvP is removed.</p>	-