



Flexible and Scalable Solution Enabling Hierarchical QoS

Traffic Management Solutions from Altera

Modern applications continue to push for network bandwidth growth. The wide variety of existing and emerging services for these applications present a broad range of quality of service (QoS) characteristics. In addition, the traffic management performance and feature requirements vary depending on the end application, the geographical region, and the operator. This drives the need for a more sophisticated, yet flexible traffic management capability to guarantee fair bandwidth allocation across all segments of the network.

Altera's traffic management solution provides a flexible and scalable platform for fast time to market. With our comprehensive device and intellectual property (IP) portfolio, you will be able to find what you need to implement your traffic management solution and differentiate yourself from your competitors .

Sophisticated Traffic Management Capability

The main bottlenecks for developing high-speed traffic management solutions are as follows:

- The need for external memory bandwidth to buffer data packets
- The need to process complex scheduling algorithms real-time in hardware

Altera provides a complete traffic management solution that addresses these challenges. Our high-performance Stratix® V FPGAs provide the performance and external memory interfaces for supporting full-duplex 40G and 100G traffic management designs. As datapath designs advance beyond 10 Gbps, the chip-to-chip interfaces moved from LVDS-based I/O standards such as SPI-4.2 to serial-based standards such as Interlaken. Stratix V FPGAs also have integrated high-speed transceivers to meet the chip-to-chip interface and the high-speed backplane requirements that reduce the overall cost and board space in the system.

For lower speed designs, such as 10G and 20G traffic management applications, you can opt for our mid-range Arria® II FPGAs. Our Arria II FPGAs provide a cost-effective solution for designs with lower performance and resource requirements.

Stratix V GX Family

Device	Logic Elements (LEs)	Transceivers (14.1 Gbps)	I/Os	Memory (Mb)
5SGXA3	340K	12, 24, 36	360 – 696	19
5SGXA4	420K	24, 36	432 – 696	37
5SGXA5	490K	24, 36, 48	432 – 840	45
5SGXA7	622K	24, 36, 48	432 – 840	50
5SGXA9	840K	36, 48	696 – 840	52
5SGXAB	952K	36, 48	696 – 840	52
5SGXB5	490K	66	432 – 600	41
5SGXB6	597K	66	432 – 600	52
5SGXB9	840K	66	600	52
5SGXBB	952K	66	600	52

Arria II GX/GZ Family

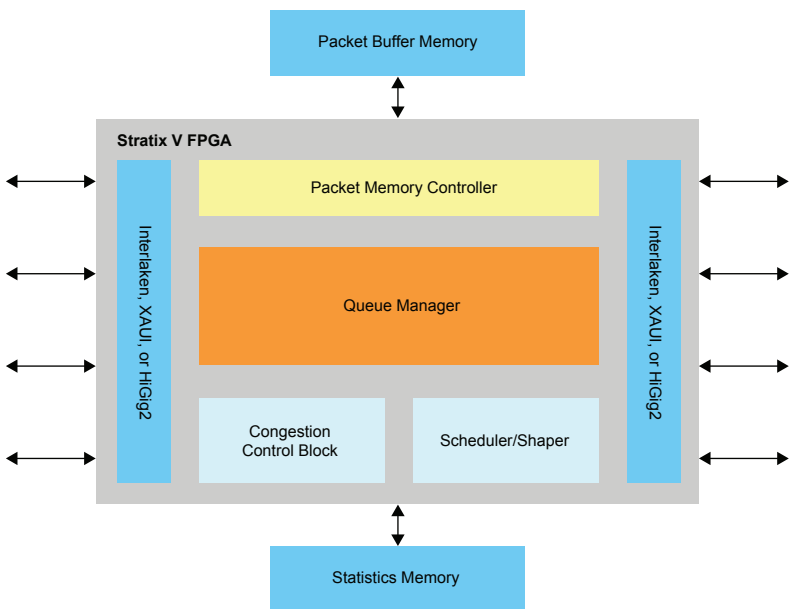
Device	LEs	Transceivers (6.375 Gbps)	I/Os	Memory (Mb)
EP2AGX45	45K	4 – 8	156 – 364	3.4
EP2AGX65	63K	4 – 8	156 – 364	5.3
EP2AGX95	94K	8 – 12	260 – 452	6.7
EP2AGX125	124K	8 – 12	260 – 452	8.1
EP2AGX190	190K	12 – 16	372 – 612	9.9
EP2AGX260	257K	12 – 16	372 – 612	11.8
EP2AGZ225	224K	16 – 24	550 – 726	11.1
EP2AGZ300	298K	16 – 24	268 – 726	14.6
EP2AGZ350	349K	16 – 24	268 – 726	16.4

The IP from Altera complements our programmable devices and helps you jump-start your design. The IP incorporates five levels of scheduling to enable you to implement hierarchical QoS, while providing flexibility for dynamic queue configuration and mapping.

Traffic Management IP Key Features

Feature	Description
Data rate	Can scale from 10G to 100G
Number of queues	Up to 256K with external memory
Number of levels	Up to five levels of scheduling
Scheduling algorithms	Strict priority (SP), round robin (RR), weighted round robin (WRR), deficit weighted round robin (DWRR), strict priority plus (SP+), and weighted fair queuing (WFQ)
Shaping algorithms	Token or leaky bucket
Congestion control	Weighted random early discard (WRED), random early discard (RED), and tail drop

Altera's Traffic Management Solution



Altera provides a modular traffic management solution with flexible interfaces to accelerate your development.

Want to Dig Deeper?

For more information about Altera's traffic management solutions, contact your Altera sales representative or FAE, or visit www.altera.com/wireline.

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