12. Power Management in Arria II Devices

AIIGX51012-3.1

This chapter describes the static and dynamic power of Arria® II devices. Static power is the power consumed by the FPGA when it is configured, but no clocks are operating. Dynamic power is composed of switching power when the device is configured and running.

The PowerPlay Power Analyzer in the Quartus® II software optimizes all designs with Arria II power technology to ensure performance is met at the lowest power consumption. This automatic process allows you to concentrate on the functionality of your design instead of the power consumption of your design.

For more information about using the PowerPlay Power Analyzer in the Quartus II software, refer to the *Power Estimation and Power Analysis* section in volume 3 of the *Quartus II Handbook*.

This chapter includes the following sections:

External Power Supply Requirements

For more information about the Arria II external power supply requirements and the power supply pin connections, refer to the following:

- For more information about Altera-recommended power supply operating conditions, refer to the *Device Datasheet for Arria II Devices* chapter.
- For more information about power supply pin connection guidelines and power regulator sharing, refer to the *Arria II Device Family Pin Connection Guidelines*.

Power-On Reset Circuitry

The Arria II power-on reset (POR) circuitry generates a POR signal to keep the device in the reset state until the power supply's voltage levels have stabilized during power-up. The POR circuitry monitors V_{CC}, V_{CCA_PLL}, V_{CCCB}, V_{CCPD}, and V_{CCIO} supplies for I/O banks 3C and 8C in Arria II GX devices, where the configuration pins are located. The POR circuitry tri-states all user I/O pins until the power supplies reach the recommended operating levels. These power supplies are required to monotonically reach their full-rail values without plateaus and within the maximum power supply ramp time (t_{RAMP}). The POR circuitry de-asserts the POR signal after the power supplies reach their full-rail values to release the device from the reset state.

The POR circuitry monitors V_{CC}, V_{CCAUX}, V_{CCCB}, V_{CCPGM}, and V_{CCPD} supplies in Arria II GZ devices. The POR circuitry keeps the Arria II GZ devices in reset state until the power supply outputs are within operating range (provided that the V_{CC} powers up fully before V_{CCAUX}).

POR circuitry is important to ensure that all the circuits in the Arria II device are at certain known states during power up. You can select the POR signal pulse width between fast POR time or standard POR time using the MSEL pin settings. For fast POR time, the POR signal pulse width is set to 4 ms for the power supplies to ramp up to full rail. For standard POR time, the POR signal pulse width is set to 100 ms for the power supplies to ramp up to full rail. In both cases, you can extend the POR time with an external component to assert the nSTATUS pin low.

For more information about the POR specification, refer to the *Device Datasheet for Arria II Devices* chapter.

For more information about MSEL pin settings, refer to the *Configuration, Design Security, and Remote System Upgrades in Arria II Devices* chapter.

Hot Socketing

Arria II I/O pins are hot-socketing compliant without the need for external components or special design requirements. Hot-socketing support in Arria II devices has the following advantages:

- You can drive the device before power up without damaging the device.
- I/O pins remain tri-stated during power up. The device does not drive out before or during power-up. Therefore, it does not affect other buses in operation.
- You can insert or remove an Arria II device from a powered-up system board without damaging or interfering with normal system and board operation.

Devices Can Be Driven Before Power-Up

You can drive signals into regular Arria II I/O pins and transceiver before or during power up or power down without damaging the device. Arria II devices support any power-up or power-down sequence to simplify the system-level designs.

I/O Pins Remain Tri-Stated During Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Arria II output buffers are turned off during system power up or power down. Also, the Arria II device does not drive out until the device is configured and working within recommended operating conditions.

Insertion or Removal of an Arria II Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

An Arria II device may be inserted into or removed from a powered up system board without damaging or interfering with system-board operation.

For Arria II GX devices, you can power up or power down the V_{CCIO}, V_{CC}, and V_{CCPD} supplies in any sequence and at any time between them. For Arria II GZ devices, you can power up or power down the V_{CC}, V_{CCIO}, V_{CCPD}, and V_{CCPGM} supplies in any sequence (provided that the V_{CC} powers up fully before V_{CCAUX}).

For more information about the hot-socketing specification, refer to the *Device Datasheet for Arria II Devices* chapter and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices* white paper.

Hot-Socketing Feature Implementation

Arria II devices are immune to latch-up when using the hot-socketing feature. The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCIO}, or V_{CCPD} power supplies for Arria II GX devices. Hot-socketing circuitry generates an internal `HOTSCKT` signal when the V_{CC}, V_{CCIO}, or V_{CCPD} power supplies for Arria II GX devices are below the threshold voltage. To support the startup current as reported by the PowerPlay Early Power Estimator (EPE) for Arria II GX devices, fully power V_{CC} before V_{CCCB} begins to ramp.

The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCIO}, V_{CCPD}, and V_{CCPGM} power supplies for Arria II GZ devices. To support the power-up sequence for all Arria II GZ devices, fully power V_{CC} before V_{CCAUX} begins to ramp.

Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuit is removed on these configuration pins to ensure that they are able to operate during configuration. Thus, it is the expected behavior for these pins to drive out during power-up and power-down sequences.

Altera uses GND as reference for the hot-socketing operation and I/O buffer designs. To ensure proper operation, Altera recommends connecting the GND between boards before connecting to the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND can otherwise cause an out-of-specification I/O voltage or current condition with the Altera® device.

Document Revision History

Table 12–1 lists the revision history for this chapter.

Table 12–1. Document Revision History

Date	Version	Changes
June 2011	3.1	■ Removed Table 1-2. ■ Updated the "Insertion or Removal of an Arria II Device from a Powered-Up System" and "Hot-Socketing Feature Implementation" sections. ■ Minor text edits.
December 2010	3.0	■ Updated for the Quartus II software version 10.1 release. ■ Added Arria II GZ devices information. ■ Minor text edits.
July 2010	2.0	Updated "Power-On Reset Circuitry" section for the Arria II GX v10.0 release.
June 2009	1.1	—
February 2009	1.0	Initial release.