Errata Sheet and Guidelines for Stratix V ES Devices

This errata sheet provides information about known device issues affecting Stratix® V engineering sample (ES) devices. It also offers guidelines you should follow when using Stratix V ES devices.

This document contains the following sections:

- "Device Errata for Stratix V ES Devices"
- "Device Guidelines for Stratix V ES Devices" on page 17

ES devices are not intended to be used for volume production.

The programming file is not compatible between ES and production devices.

Device Errata for Stratix V ES Devices

Table 1 lists the specific device issues and the affected Stratix V ES devices.

Table 1. Device Issues (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"Analog-to-Digital Converter Temperature Sensing Diode (ADCTSD) Feature" Stratix V ES devices will not support the ADCTSD feature.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"GX Transmitter Buffer Voltage Sensitivity" If you are using one of the power supply voltage combinations listed in Table 2, contact mySupport.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"External Memory Interface Fitter Error" With external memory interface designs, the Quartus® II software may issue a no-fit message.	5SGXA7 ES, 5SGTC7 ES	Production Devices
"BER Count in 10GBASE-R PHY IP" The `BER_COUNT` register of the 10GBASE-R PHY IP may continue incrementing beyond 16 in a 125 µs window.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"Fractional PLL Clock Switchover" If you have enabled the Manual Fractional PLL Clock Switchover feature, if both the reference and backup clocks are toggling prior to completion of the configuration, the fractional PLL starts with the backup clock.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"DQ/DQS Pin Mapping Issue" The pin table for the 5SGXB6 ES device on www.altera.com (revision 1.0) and in the Quartus II software prior to version 11.1 FAE Beta has incorrect DQ and DQS assignments.	5SGXB6 ES	Production Devices

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Table 1. Device Issues (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"Transceiver refclk Inversion" The clock signal from the dedicated transceiver `refclk` into the FPGA fabric is inverted.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"ATX PLL Clock Divider" The ATX PLL has limitations. If one of the two conditions specified in this issue is true, contact mySupport.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"Configuration via Protocol (CvP) Using Gen2" CvP initialization-and-update mode and CvP-update mode will not be supported at PCI Express® (PCIe®) Gen 2 data rates in ES silicon.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"I/O Pin Leakage Current"	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"Power and Performance" Certain power supplies must be increased.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"Required Power Sequencing" Follow the required power up sequencing.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"V_{CCHIP} Power Pin Connection" V_{CCHIP} cannot be powered down.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"nIO_PULLUP Connection" The `nIO_PULLUP` pin must be connected to GND.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	None
"Clock Network Restrictions" The input reference clock frequency for the top and bottom fractional PLL when using a global or regional clock is limited to 400 MHz.	5SGXA7 ES, 5SGTC7 ES	Production Devices
"Clock Input Support" Global and regional clock networks are limited to an f_{MAX} of 400 MHz when you use the clock pins directly without a PLL.	5SGXA7 ES, 5SGTC7 ES	Production Devices
"x4 DQS Group Support" Some of the x4 DQS groups are not available.	5SGXA7 ES, 5SGTC7 ES	Production Devices
"PCIe Gen3 Support, CRC with Error Detection, Partial Reconfiguration, or Scrubbing Features" If you need any of these features, contact mySupport.	5SGXA7 ES, 5SGTC7 ES	Production Devices
"JTAG Port Access Limitation After Configuration" If you use FPP, PS, or AS as a primary configuration scheme, you will not be able to access the JTAG ports after configuration completes, unless you issue the JTAG FACTORY command before configuration.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices
"LVDS DPA and Soft CDR Support" There are limitations with LVDS DPA and soft CDR support. For more information, contact mySupport.	5SGXA7 ES, 5SGTC7 ES, 5SGXB6 ES	Production Devices

Analog-to-Digital Converter Temperature Sensing Diode (ADCTSD) Feature

Stratix V ES devices will not support the ADCTSD feature. Altera recommends using an external temperature sensing diode (TSD) for device thermal management of Stratix V ES devices.

GX Transmitter Buffer Voltage Sensitivity

If you are using one of the power supply voltage combinations listed in Table 2, contact mySupport for the correct version of the Quartus II software to ensure proper setting and operation of the GX transmitter buffers.

Table 2. Conditions affecting the GX Transmitter Buffer

Condition	V_{CCA_GXB}	V_{CCH_GXB}	Affected
Data rate > 6.5G TX PLL = CMU PLL	3.0 V ± 100 mv	1.6 V ± 50mV	Yes
Data rate = All TX PLL = ATX PLL	3.3 V ± 100 mv	1.6 V ± 50mV	Yes

External Memory Interface Fitter Error

With external memory interface designs, the Quartus II software may issue the following no-fit error message:

```
Fitter error: The DQS Group fed by DQS I/O pin, may not function correctly
on the selected Stratix V ES Device
```

A register transfer level (RTL) workaround may be available to bypass this Fitter error; however, contact mySupport to ensure that you have the latest version of the Quartus II software that resolves this Fitter error.

BER Count in 10GBASE-R PHY IP

The `BER_COUNT` register of the 10GBASE-R PHY IP may continue incrementing beyond 16 in a 125 µs window. There is no impact on the bit error rate (BER) monitor block or the `hi_ber` status flag.

Fractional PLL Clock Switchover

If you have enabled the Manual Fractional PLL Clock Switchover feature and if both the reference and backup clocks are toggling prior to completion of the configuration, the fractional PLL starts with the backup clock. To avoid having the fractional PLL start with the backup clock, gate the reference and backup clocks until the part enters user mode (optionally indicated through `INIT_DONE`), or engage the clock switchover circuitry to switch to the reference clock (for example, toggling the fractional PLL's `extclkswitch` input).

DQ/DQS Pin Mapping Issue

The pin table for the 5SGXB6 ES device on www.altera.com (revision 1.0) and in the Quartus II software earlier than version 11.1 FAE Beta has incorrect DQ and DQS assignments. The incorrect DQ and DQS assignments have been fixed in version 1.1 of the pin table on www.altera.com and in the Quartus II software version 11.1 FAE Beta or later.

To ensure that your DQ and DQS pin assignments are correct, recompile your design in the Quartus II software version 11.1 or later.

Transceiver refclk Inversion

The clock signal from the dedicated transceiver `refclk` into the FPGA fabric is inverted. If your design uses the dedicated transceiver `refclk` pins to drive logic in the FPGA fabric, or as an input reference clock into the fractional PLL, you must add the following constraint to the Synopsys Design Constraint (**.sdc**) file used by the TimeQuest Timing Analyzer:

```
create_generated_clock -name <name> -source [get_ports <refclk_port_name>]
-invert [get_pins -compatibility_mode <refclk_port_name>~*outclk]
```

For example:

```
create_generated_clock -name refclk_inverted -source [get_ports refclk]
-invert [get_pins -compatibility_mode refclk~*outclk]
```

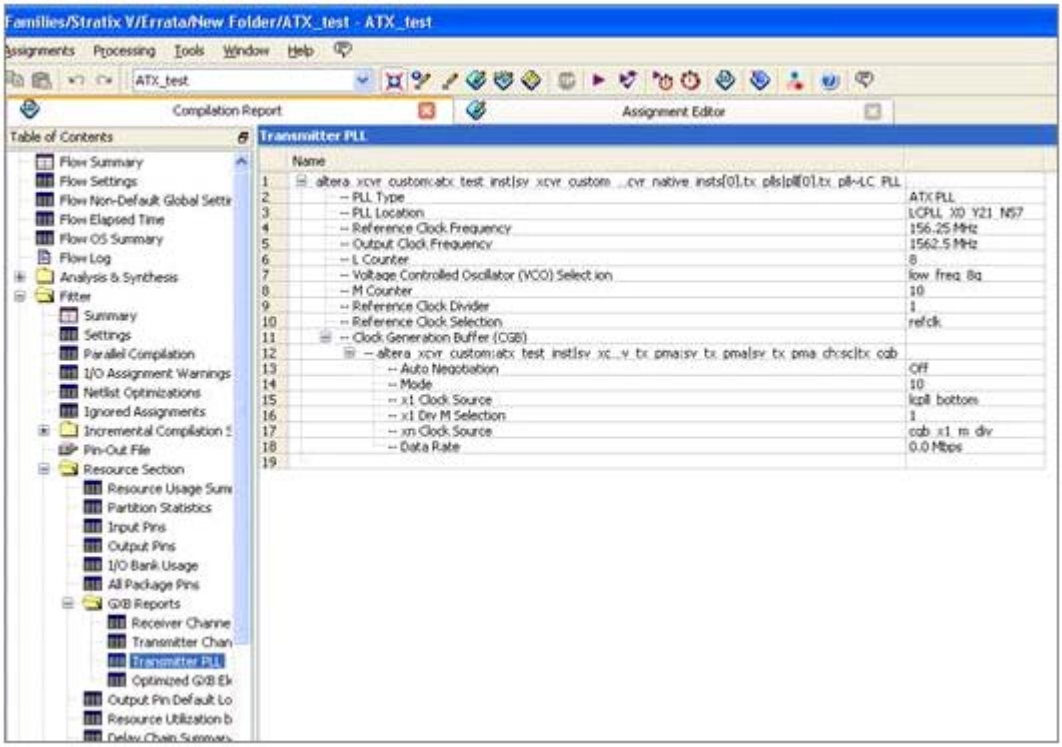
ATX PLL Clock Divider

The auxiliary transmit (ATX) PLL has limitations. If either one of the following conditions is true, contact mySupport:

- In 5SGXA7 ES and 5SGTC7 ES devices, the L counter setting is 1, 4, or 8
- In all ES devices, the L counter setting is 2 and the output clock frequency is > 5.2 GHz

You can obtain information about the output clock frequency and L counter settings from the Fitter report. To view this information, select **Fitter** report, then **Resource Section**, **GXB Reports**, and lastly **Transmitter PLL**, as shown in Figure 1.

Figure 1. Fitter Report, Transmitter PLL Page



Configuration via Protocol (CvP) Using Gen2

CvP-initialization-and-update mode and CvP-update mode will not be supported at PCIe Gen 2 data rates in ES silicon.

I/O Pin Leakage Current

Refer to the *Stratix V Device Datasheet*.

Power and Performance

Altera recommends using adjustable or programmable power regulators on all power rails in case the voltage rails need to be boosted to achieve the highest performance. Table 3 through Table 5 list the power supplies that must be raised. Table 6 lists a reference guide for the Stratix V ES required power supply and power sequence diagrams.

Power consumption on the ES devices may also be higher than target. Altera recommends using the ES Max Power models to estimate design power consumption for ES devices. For more information about how the PowerPlay Early Power Estimator (EPE) is affected by this increase, contact mySupport.

Battery life on circuits powered by V_{CCBAT} may be less than 10 years.

Table 3 lists the power supply change requirements for 5SGXA7 ES devices.

Table 3. Power Supply Change Requirements for 5SGXA7 ES Devices

Voltage Supply Name	Datasheet Specification	Requirement
V_{CC}, V_{CCHSSI}, V_{CCHIP}	0.85 V	0.9 V ± 30 mV
V_{CCA_GXB}	2.5 V (≤ 6.5 Gbps) 3.0 V (> 6.5 Gbps)	2.5 V ± 100 mv (≤ 6.5 Gbps and ATX PLL is **not** being used) 3.0 V ± 100 mv (> 6.5 Gbps and ATX PLL is **not** being used) 3.3 V ± 100 mv (all data rates when ATX PLL **is** being used)
V_{CCR_GXB}, V_{CCT_GXB}	0.85 V (≤ 6.5 Gbps) 1.0 V (> 6.5 Gbps)	0.9 V ± 30 mV (≤ 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (> 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (all data rates when ATX PLL **is** being used)
V_{CCH_GXB}	1.5 V ± 5%	1.5 V ± 50 mV (≤ 6.5 Gbps and ATX PLL is **not** being used) 1.6 V ± 50 mV (> 6.5 Gbps and ATX PLL is **not** being used) 1.6 V ± 50 mV (all data rates when ATX PLL **is** being used)

Table 4 lists the power supply change requirements for 5SGTC7 ES devices.

Table 4. Power Supply Change Requirements for 5SGTC7 ES Devices

Voltage Supply Name	Datasheet Specification	Requirement
V_{CC}, V_{CCHSSI}, V_{CCHIP}	0.85 V	0.9 V ± 30 mV
V_{CCA_GXB}, V_{CCA_GTB}	3.0 V	3.3 V ± 100 mv
V_{CCR_GXB}, V_{CCT_GXB}	0.85 V (≤ 6.5 Gbps) 1.0 V (> 6.5 Gbps)	0.9 V ± 30 mV (≤ 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (> 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (all data rates when ATX PLL **is** being used)
V_{CCH_GXB}	1.5 V ± 5%	1.6 V ± 50 mV
V_{CCR_GTB}, V_{CCT_GTB}, V_{CCL_GTB}	1.0 V ± 5%	1.25 V ± 30 mV

Table 5 lists the power supply change requirements for 5SGXB6 ES devices.

Table 5. Power Supply Change Requirements for 5SGXB6 ES Devices

Voltage Supply Name	Datasheet Specification	Requirement
V_{CC}, V_{CCHSSI}, V_{CCHIP}	0.85 V	0.9 V ± 30 mV
V_{CCA_GXB}	2.5 V (≤ 6.5 Gbps) 3.0 V (> 6.5 Gbps)	2.5 V ± 100 mv (≤ 6.5 Gbps and ATX PLL is **not** being used) 3.0 V ± 100 mv (> 6.5 Gbps and ATX PLL is **not** being used) 3.3 V ± 100 mv (all data rates when ATX PLL **is** being used)
V_{CCR_GXB}, V_{CCT_GXB}	0.85 V (≤ 6.5 Gbps) 1.0 V (> 6.5 Gbps)	0.9 V ± 30 mV (≤ 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (> 6.5 Gbps and ATX PLL is **not** being used) 1.2 V ± 30 mV (all data rates when ATX PLL **is** being used)
V_{CCH_GXB}	1.5 V ± 5%	1.5 V ± 50 mV (≤ 6.5 Gbps and ATX PLL is **not** being used) 1.6 V ± 50 mV (> 6.5 Gbps and ATX PLL is **not** being used) 1.6 V ± 50 mV (all data rates when ATX PLL **is** being used)

Table 6 lists a reference guide for the required power supply and power sequencing diagrams for all Stratix V ES devices.

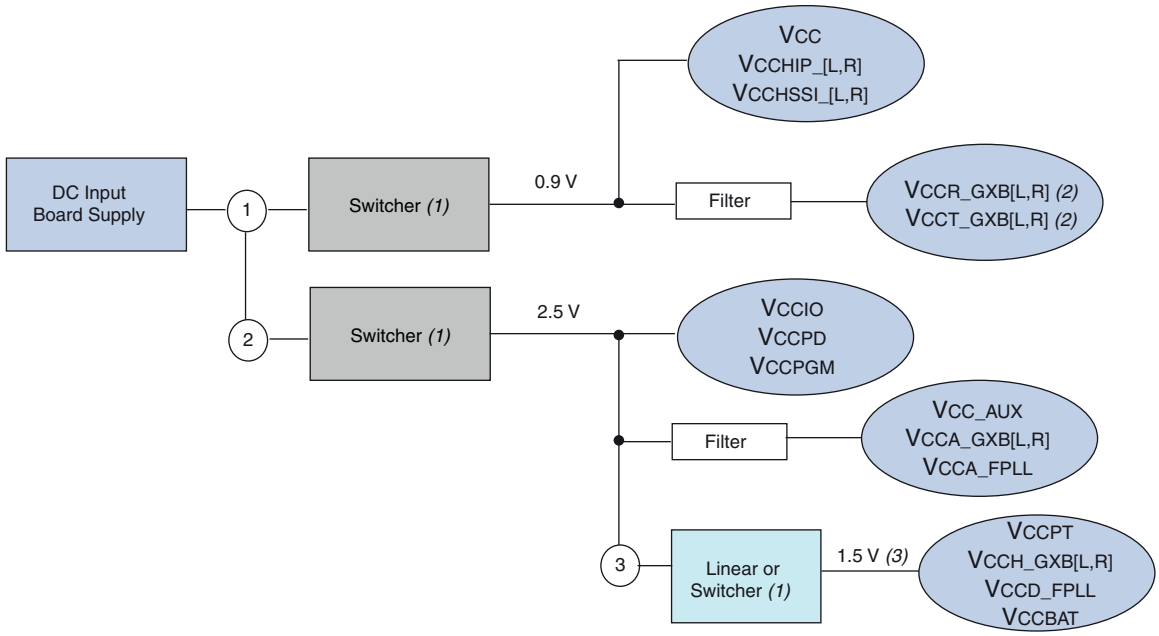
Table 6. Reference to the Stratix V Required Power Supplies and Power Sequencing Diagrams

Device	Condition	Power Supply Diagram	Power Sequencing Diagram
5SGXA7 ES	Data Rate ≤ 6.5 Gbps for the CMU PLL and the ATX PLL is **not** being used	Figure 2	Figure 7
	Data Rate > 6.5 Gbps for the CMU PLL or any data rate using the ATX PLL	Figure 4	Figure 9
5SGXB6 ES	Data Rate ≤ 6.5 Gbps for the CMU PLL and the ATX PLL is **not** being used	Figure 2	Figure 7
	Data Rate > 6.5 Gbps for the CMU PLL or any data rate using the ATX PLL	Figure 5	Figure 10
5SGTC7 ES	Data Rate ≤ 6.5 Gbps for the CMU PLL and the ATX PLL is **not** being used	Figure 3	Figure 8
	Data Rate > 6.5 Gbps for the CMU PLL or any data rate using the ATX PLL	Figure 6	Figure 11

Figure 2 shows the resulting power supply block diagram example for transceivers with data rates ≤ 6.5 Gbps and not using the ATX PLL.

In this example, $V_{CCR\_GXB\ [L,\ R]}$ and $V_{CCT\_GXB\ [L,\ R]}$ can be supplied with 0.85-, 0.9-, or 1.2-V power supply.

Figure 2. Example Power Supply Block Diagram for Transceivers with Data Rates ≤ 6.5 Gbps for the CMU PLL and not Using the ATX PLL (5SGXA7 ES and 5SGXB6 ES Devices)



Notes to Figure 2:

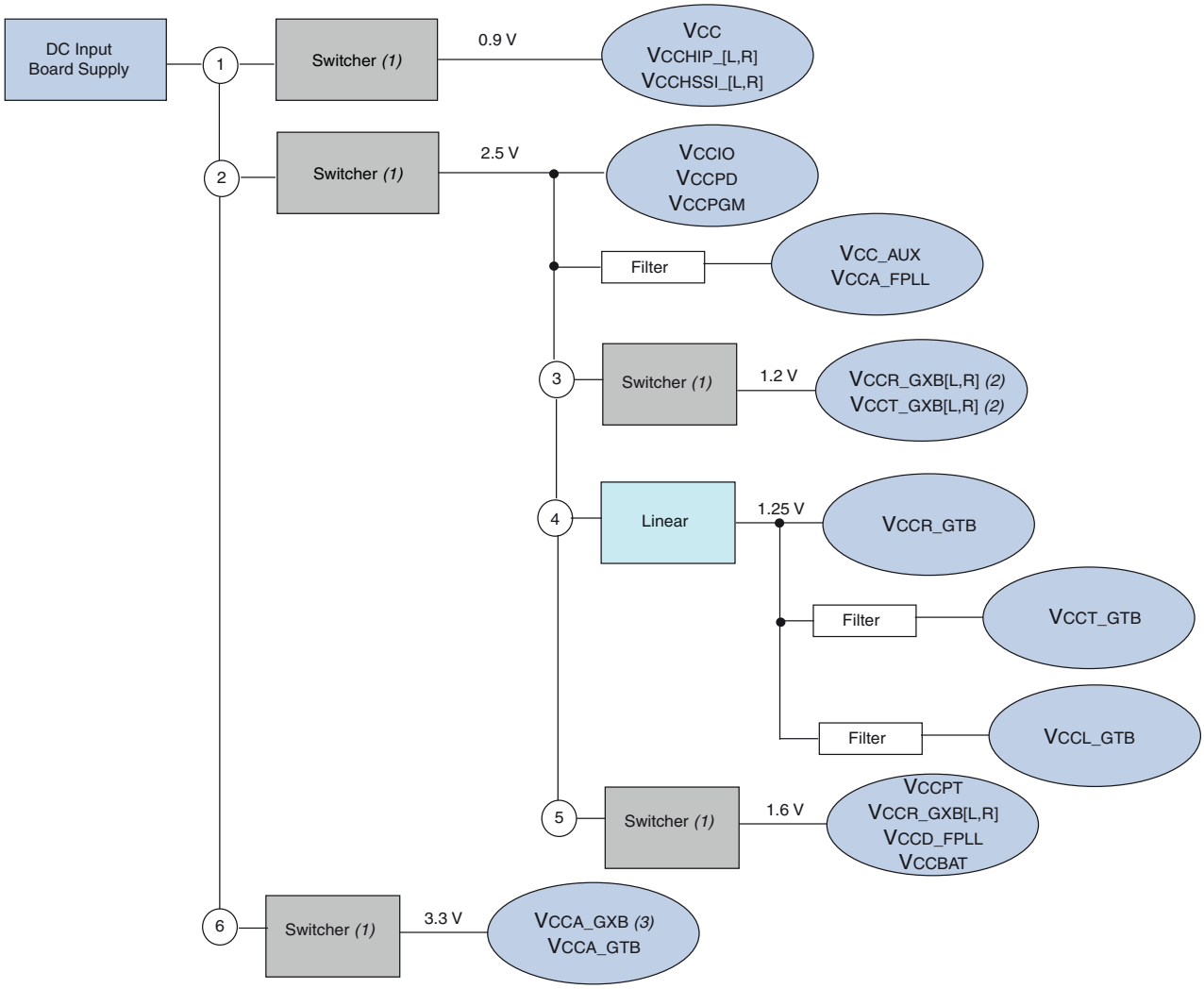
(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher (a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has a fast transient response with a line regulation < 0.4% and load regulation < 1.2%).

(2) You can connect the `VCCR_GXB[L,R]` and `VCCT_GXB[L,R]` pins to a 0.9- or 1.2-V power supply when the data rate is ≤ 6.5 Gbps and you are using only CMU PLLs.

(3) You can connect the `VCCH_GXB[L,R]`, `VCCPT`, `VCCD_FPLL`, and `VCCBAT` pins to a 1.5- or 1.6-V power supply when the data rate is ≤ 6.5 Gbps and you are using only CMU PLLs.

Figure 3 shows the resulting power supply block diagram example for transceivers with data rates ≤ 6.5 Gbps and not using the ATX PLL.

Figure 3. Example Power Supply Block Diagram for Transceivers with Data Rates ≤ 6.5 Gbps for the CMU PLL and not Using the ATX PLL (5SGTC7 ES Devices)



Notes to Figure 3:

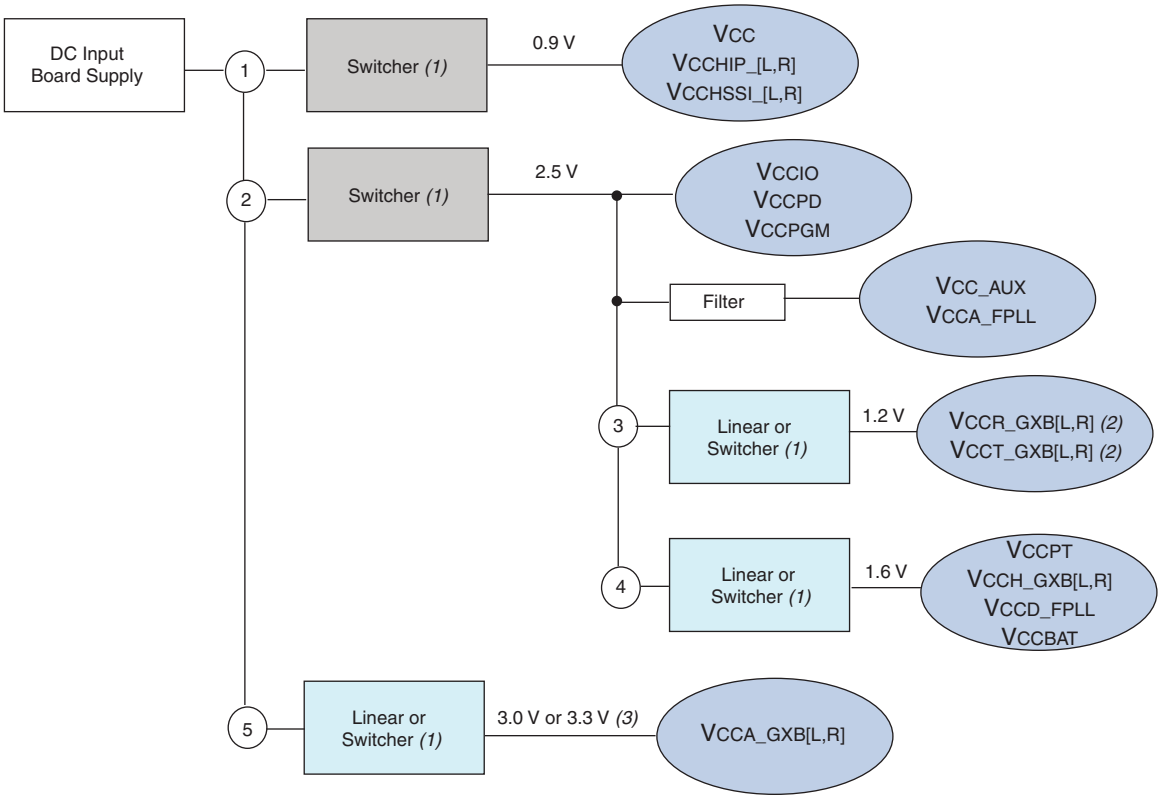
(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher (a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has a fast transient response with a line regulation < 0.4% and load regulation < 1.2%).

(2) You can connect the `VCCR_GXB[L,R]` and `VCCT_GXB[L,R]` pins to a 0.9- or 1.2-V power supply when the data rate is ≤ 6.5 Gbps and you are using only CMU PLLs.

(3) You can connect the `VCCA_GXB[L,R]` pins to a 2.5-, 3.0-, or 3.3-V power supply if you do not use the ATX PLL. If you use the ATX PLL, you must connect the `VCCA_GXB[L,R]` pins to 3.3 V.

Figure 4 shows the resulting power supply block diagram example for transceivers with data rates > 6.5 Gbps for the CMU PLL or any data rate using the ATX PLL for 5SGXA7 ES devices.

Figure 4. Example Power Supply Block Diagram for Transceivers with Data Rate > 6.5 Gbps for the CMU PLL or any Data Rate Using the ATX PLL (5SGXA7 ES Devices)



Notes to Figure 4:

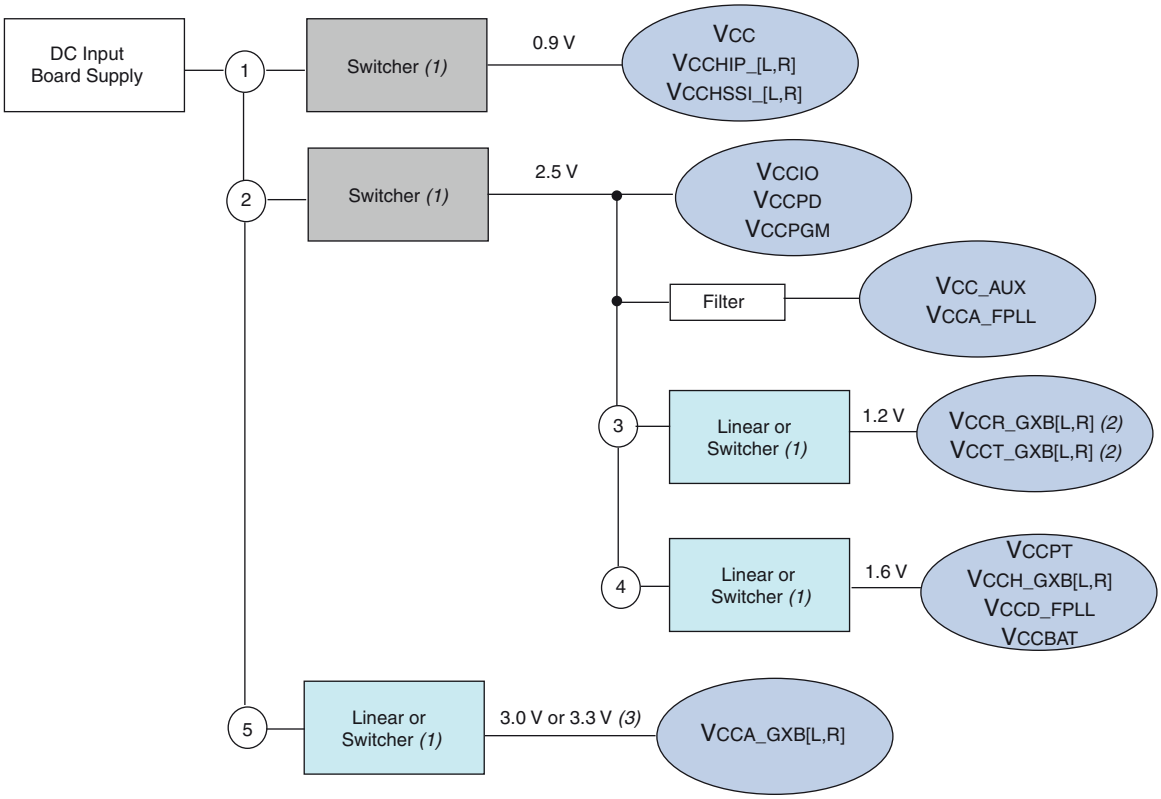
(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher (a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has a fast transient response with a line regulation < 0.4% and load regulation < 1.2%).

(2) Although `VCCR_GXB` and `VCCT_GXB` may share a regulator, for better performance, these power supplies must be isolated from each other with at least 40-dB isolation.

(3) If your design uses only CMU PLLs, you can connect the `VCCA_GXB[L,R]` pins to either 3.0 or 3.3 V. If you use the ATX PLL, the `VCCA_GXB[L,R]` pins must be connected to 3.3 V.

Figure 5 shows the resulting power supply block diagram example for transceivers with data rates > 6.5 Gbps and not using the ATX PLL or for all data rates when using the ATX PLL for 5SGXB6 ES devices.

Figure 5. Example Power Supply Block Diagram for Transceivers with Data Rates > 6.5 Gbps and not Using the ATX PLL or for All Data Rates when Using the ATX PLL (5SGXB6 ES Devices)



Notes to Figure 5:

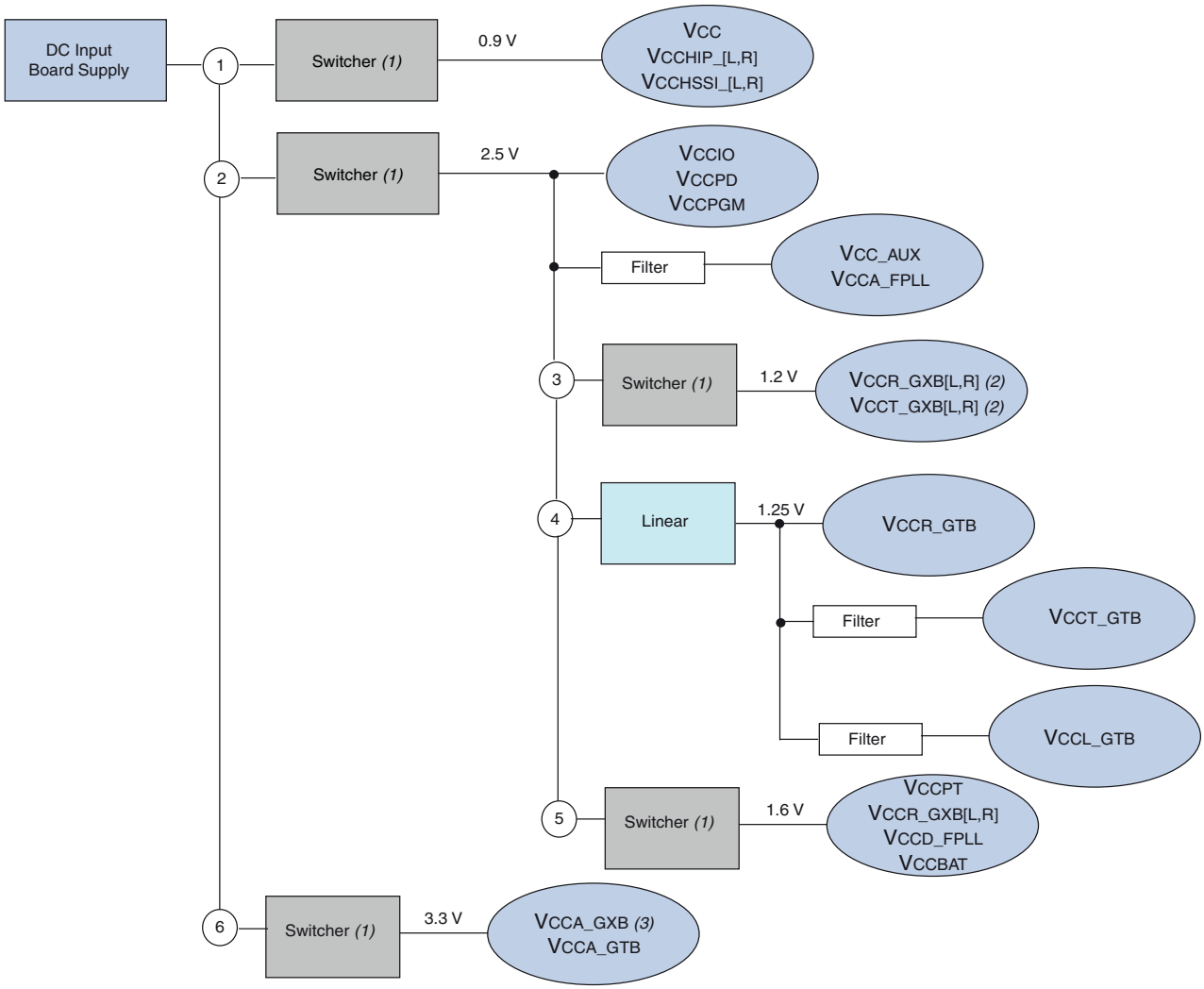
(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher (a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has a fast transient response with a line regulation < 0.4% and load regulation < 1.2%).

(2) Although `VCCR_GXB` and `VCCT_GXB` may share a regulator, for better performance, these power supplies must be isolated from each other with at least 40-dB isolation.

(3) If you do not use the ATX PLL, you can connect the `VCCA_GXB[L,R]` pins to either 3.0 or 3.3 V. If you use the ATX PLL, the `VCCA_GXB[L,R]` pins must be connected to 3.3 V.

Figure 6 shows the resulting power supply block diagram example for transceivers with data rates > 6.5 Gbps and not using the ATX PLL or for all data rates when using the ATX PLL.

Figure 6. Example Power Supply Block Diagram for Transceivers with Data Rates > 6.5 Gbps for the CMU PLL and not Using the ATX PLL (5SGTC7 ES Devices)



Notes to Figure 6:

(1) When using a switcher to supply these voltages, the switcher must be a low noise switcher (a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has a fast transient response with a line regulation < 0.4% and load regulation < 1.2%).

(2) You can connect the `VCCR_GXB[L,R]` and `VCCT_GXB[L,R]` pins to a 0.9- or 1.2-V power supply when the data rate is ≤ 6.5 Gbps and you are using only CMU PLLs.

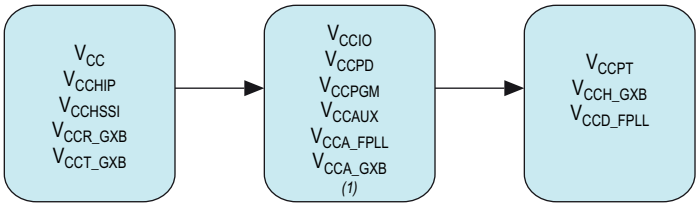
(3) You can connect the `VCCA_GXB[L,R]` pins to a 2.5-, 3.0-, or 3.3-V power supply if you do not use the ATX PLL. If you use the ATX PLL, you must connect the `VCCA_GXB[L,R]` pins to 3.3 V.

Required Power Sequencing

The following power-up sequence must be followed to ensure proper power up. Failure to follow the required power sequencing may result in additional current consumption or functionality issues.

Figure 7 through Figure 11 show the updated power sequencing.

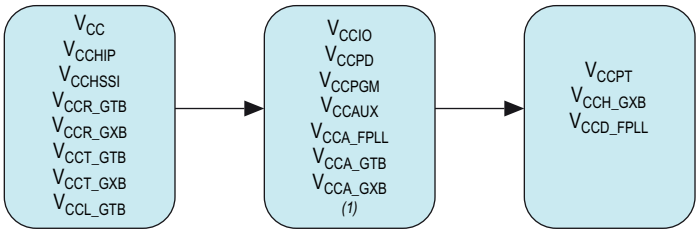
Figure 7. Required Power Sequencing (5SGXA7 ES and 5SGXB6 Devices) for Data Rates ≤ to 6.5 Gbps Using the CMU PLL and Without Using the ATX PLL



Note to Figure 7:

(1) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board) or in any sequence after V_{CCPGM}.

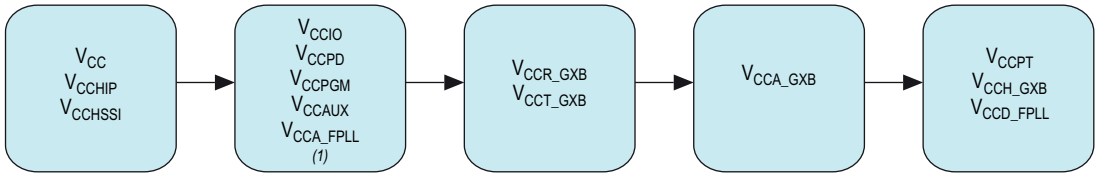
Figure 8. Required Power Sequencing (5SGTC7 ES Devices) for Data Rates ≤ to 6.5 Gbps Using the CMU PLL and Without Using the ATX PLL



Note to Figure 8:

(1) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board) or in any sequence after V_{CCPGM}.

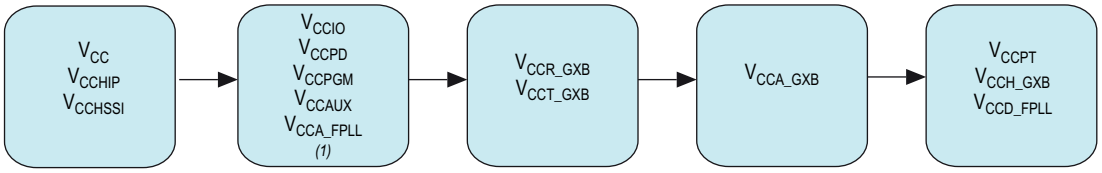
Figure 9. Required Power Sequencing (5SGXA7 ES Devices) for Data Rates > 6.5 Gbps Using the CMU PLL and All Data Rates Using the ATX PLL



Note to Figure 9:

(1) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board) or in any sequence after V_{CCPGM}.

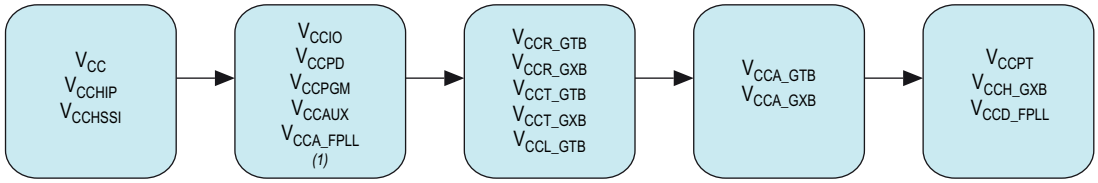
Figure 10. Required Power Sequencing (5SGXB6 ES Devices) for Data Rates > 6.5 Gbps Using the CMU PLL and All Data Rates Using the ATX PLL



Note to Figure 10:

(1) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board) or in any sequence after V_{CCPGM}.

Figure 11. Required Power Sequencing (5SGTC7 ES Devices) for Data Rates > 6.5 Gbps Using the CMU PLL and All Data Rates Using the ATX PLL



Note to Figure 9:

(1) Power up V_{CCPGM} first. V_{CCIO} and V_{CCPD} can be powered up together with V_{CCPGM} (if these supplies share a common plane or traces on the board) or in any sequence after V_{CCPGM}.

V_{CCHIP} Power Pin Connection

V_{CCHIP} cannot be powered down. You must connect V_{CCHIP} to a 0.9-V power supply for all designs.

nIO_PULLUP Connection

The `nIO_PULLUP` pin must be connected to GND. The weak pull-up resistor on the user I/O and dual-purpose I/O pins is enabled before and during configuration. Because of this connection, there will be an increase in current if another device is driving the I/O pins during configuration, but the increase amount is negligible.

Clock Network Restrictions

If you use a global or regional clock network to drive the top or bottom fractional PLLs, the f_{MAX} is limited to 400 MHz (the specification is 717 MHz).

Clock Input Support

Global and regional clock networks are limited to an f_{MAX} of 400 MHz (the specification is 717 MHz) when you use the clock pins directly without using a PLL. Use a PLL if the f_{MAX} for the clock is greater than 400 MHz.

x4 DQS Group Support

Some of the x4 DQ strobe (DQS) groups are not available. If you require x4 DQS group support, contact mySupport.

PCIe Gen3 Support, CRC with Error Detection, Partial Reconfiguration, or Scrubbing Features

If you require the cyclic redundancy check (CRC) with error detection, partial reconfiguration, or scrubbing features, or are planning to implement a PCIe Gen3 interface, contact mySupport.

JTAG Port Access Limitation After Configuration

If you use fast passive parallel (FPP), passive serial (PS), or active serial (AS) as your Stratix V ES primary configuration scheme, you will not be able to access the JTAG ports after configuration completes. You cannot access the JTAG ports because Stratix V ES devices power up in secure mode, allowing only mandatory JTAG 1149.1 instructions after power-on reset (POR). Therefore, you will not be able to use SignalTap™ II Logic Analyzer, System Console, or Sources and Probes when using any one of the above-mentioned configuration schemes, unless you issue the JTAG FACTORY instruction after the device exits POR and before configuration begins.

☞ You must issue the JTAG FACTORY instruction after each powerup because powering down and powering up the device puts the device back into secure mode.

To issue the JTAG FACTORY instruction, your PCB design must accommodate the appropriate access on the `nCONFIG` pin to pull the signal to GND or to release it high at anytime. One way to accommodate access on the `nCONFIG` pin is to have a two-way connector pin that connects the `nCONFIG` pin to GND or to a 10-kΩ pull-up resistor to V_{CCPGM}.

To issue the JTAG FACTORY instruction, follow these steps:

1. After powerup, hold the `nCONFIG` pin low to prevent the device from configuring in FPP, PS, or AS mode.
2. Using the JTAG interface, shift in the 10-bit FACTORY instruction JTAG code.
3. Reset the JTAG tap state machine and continue to clock the `TCK` pin for 200 clock cycles.

   You can execute steps 2 and 3 using a JAM (**.jam**) file and the Quartus_jli or JAM Player tool.

   For more information about how to issue the JTAG FACTORY instruction, refer to the *JTAG Boundary-Scan Testing in Stratix V Devices* chapter in the *Stratix V Device Handbook*.

Example 1 shows an example **.jam** file.

Example 1.

```
ACTION ISSUE_FACTORY = EXECUTE;
PROCEDURE EXECUTE;
BOOLEAN X = 0;
DRSTOP IDLE;
IRSTOP IDLE;
STATE IDLE;
IRSCAN 10, $281;
DRSCAN 32, $FFFFFFFF;
STATE RESET;
WAIT IDLE, 200 CYCLES;
STATE IDLE;
EXIT 0;
ENDPROC;
```

Execute the **.jam** in Example 1 with the following command:

quartus_jli -c<*cable*> -aISSUE_FACTORY <*jamfile_name*>.jam

jam.exe -aISSUE_FACTORY <*jamfile_name*>.jam

4. Release nCONFIG high. After a period of time denoted by the t_{CF2ST1} timing parameter, nSTATUS is released high.

For information about the t_{CF2ST1} timing parameter, refer to the *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices* chapter in the *Stratix V Device Handbook*.

After nSTATUS is released high, the device is released from secure mode and all the JTAG instructions are enabled. You can then perform JTAG programming or use any of the on-chip debugging features (SignalTap II Logic Analyzer, SystemConsole, or Sources and Probes).

For devices set up in the JTAG scheme only, you do not need to set up the FACTORY instruction separately. The Quartus II software automatically issues the FACTORY instruction during JTAG programming when using the Quartus II programmer or Quartus_jli. The FACTORY instruction is also incorporated into Jam™ Standard Test and Programming Language (STAPL) (**.jam**), JAM Byte Code File (**.jbc**), or Serial Vector Format (**.svf**) files.

LVDS DPA and Soft CDR Support

There are limitations with LVDS dynamic phase alignment (DPA) and soft clock data recovery (CDR) support. For more information, contact mySupport.

Device Guidelines for Stratix V ES Devices

The following section describes guidelines you should follow when using Stratix V ES devices.

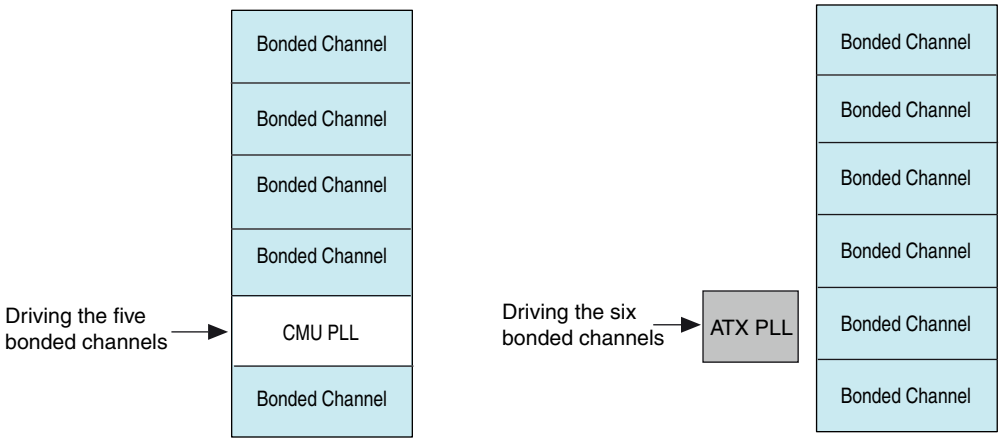
Adjustable Power Regulator

Altera recommends using adjustable or programmable power regulators on all power rails in case voltage rails need to be boosted to achieve the highest performance.

Bonded Channels Must be Contiguous

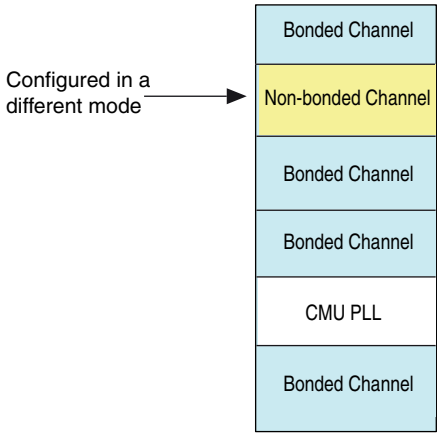
Bonded channels must be contiguous. Figure 12 shows an example of supported configurations.

Figure 12. Bonded Channels Using a CMU PLL or a ATX PLL—Supported Configurations



Bonding across non-bonded channels is not allowed unless the channel is configured as a CMU PLL. Figure 13 shows an example of a non-supported configuration.

Figure 13. Bonded Channels—Non-Supported Configuration



External Memory Interfaces Pin Placement

To help close timing at or above 400 MHz, follow the recommended pin placement guidelines.

Document Revision History

Table 7 lists the revision history for this errata sheet.

Table 7. Document Revision History

Date	Version	Changes
December 2014	1.7	■ Changed the Planned Fix status for the following sections: ■ "I/O Pin Leakage Current" ■ "nIO_PULLUP Connection" ■ Changed the description for the "I/O Pin Leakage Current" section.
January 2012	1.6	■ Added the "Analog-to-Digital Converter Temperature Sensing Diode (ADCTSD) Feature" section. ■ Added the "GX Transmitter Buffer Voltage Sensitivity" section. ■ Updated Example 1. ■ Updated the VCCA_GXB voltage requirement in Table 3, Table 4, and Table 5.
November 2011	1.5	■ Updated the "ATX PLL Clock Divider", "Fractional PLL Clock Switchover", "Power and Performance", and "Required Power Sequencing" sections. ■ Minor text edits.
October 2011	1.4	■ Added the "External Memory Interface Fitter Error", "BER Count in 10GBASE-R PHY IP", "Fractional PLL Clock Switchover", and "DQ/DQS Pin Mapping Issue" sections. ■ Minor text edits.
September 2011	1.3	■ Updated the "Power and Performance", "Required Power Sequencing", "Clock Input Support", and "LVDS DPA and Soft CDR Support" sections. ■ Updated Table 1. ■ Minor text edits.
August 2011	1.2	■ Added the "Transceiver refclk Inversion", "ATX PLL Clock Divider", "Configuration via Protocol (CvP) Using Gen2", and "I/O Pin Leakage Current" sections to the Device Errata for Stratix V ES Devices section. ■ Updated the "Power and Performance" and "Required Power Sequencing" sections.
July 2011	1.1	■ Corrected a typo in the "Increased Power Supply Voltage Levels" and "Required Power Sequencing" sections. ■ Added the "Bonded Channels Must be Contiguous" and "External Memory Interfaces Pin Placement" sections to the Device Guidelines for S*tratix V ES Devices* section.
June 2011	1.0	Initial release.