Digital Channelizer + 3.0 GSPS dual channel ADC Example Design

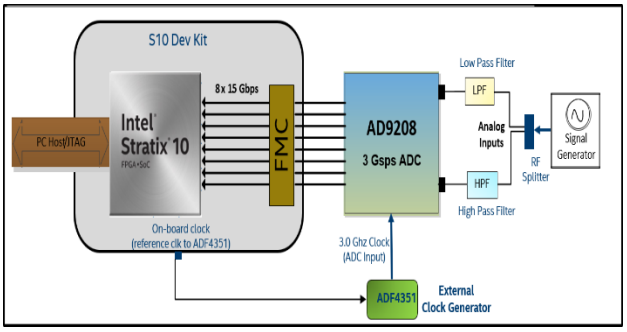
1.0 Example Design

Description

Channelizer is a wideband receiver that splits a wide bandwidth into smaller ones to separate signals of interests from noise and interferers so that low SNR signals can be reliably detected in individual subchannels. It channelizes the wide bandwidth to separate signals of interest through a filter bank and Fast Fourier Transform (FFT).

Intel® has developed a highly parameterizable and efficient super-sample rate FFT IP. This allows the designer to select the number of phases and size of the FFT for DSP Builder for Intel® FPGA to output an efficient implementation for GHz sample rate Analog to Digital Converters (ADCs). In addition, it shows the efficient implementation of FFT for real input, by utilizing half-length transform.

To demonstrate this capability, Intel® has incorporated Analog Devices™ 3Gsps 14-bit dual channel, under-sampling ADC- AD9208 using JESD204B interface. The reference design displays various channels in Matlab® via Intel® system-in-the-loop feature.

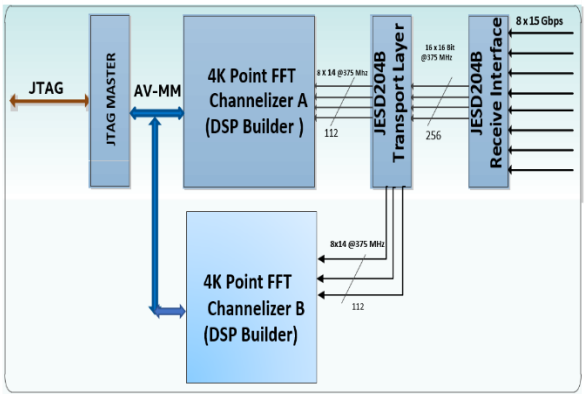


Features

- Programmable super sample rate FFT IP
- Programmable Poly-Phase Filter-Bank IP
- Half-Length FFT Optimization for Real Input Samples
- Intel® FPGA-in-the-Loop with MATLAB
- JESD204B interface to Analog Devices™ 3GSps 14-bit dual channel ADC- AD9208 through FMC
- Intel® Stratix® 10 GX FPGA Development Kit

Applications

- Wideband Communication Systems
- Cable system
- Measurement equipment



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