

OTU2 I.9 FEC IP Core (IP-OTU2EFECI9) Data Sheet

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1 Introduction

The Altera G.975 I.9, IP-OTU2EFECI9 IP core implements two interleaved BCH (1020, 988) super FEC code from the appendix I.9 of the ITU-T G.975.1 standard, [1].

The main features are:

- Net electrical coding gain (NECG) of ~8.5 dB
- 7% overhead
- Latency of 144 μ sec (includes both encoder + decoder latency)
- 64 bit data path width
- Error statistics monitoring:
 - Counts of corrected errors
 - Counts of uncorrectable component codes
 - Counts of corrected zeros relative to corrected ones

2 Architecture

Figure 1 illustrates the system architecture of the IP-OTU2EFECI9 IP core.

The FEC encoder receives OTU2 data including frame alignment signal (FAS) and multi-frame alignment signal (MFAS) from the device core. The OTU2 data is encoded with redundant FEC data. The resulting FEC encoded OTU2 must subsequently be scrambled before it is transmitted across the OTN network.

In the other direction the frame start of the OTU2 received from the OTN network must be recovered in order to forward the descrambled OTU2 data to the FEC decoder. The redundant FEC data is decoded and identified errors are corrected before the data is forwarded to the device core.

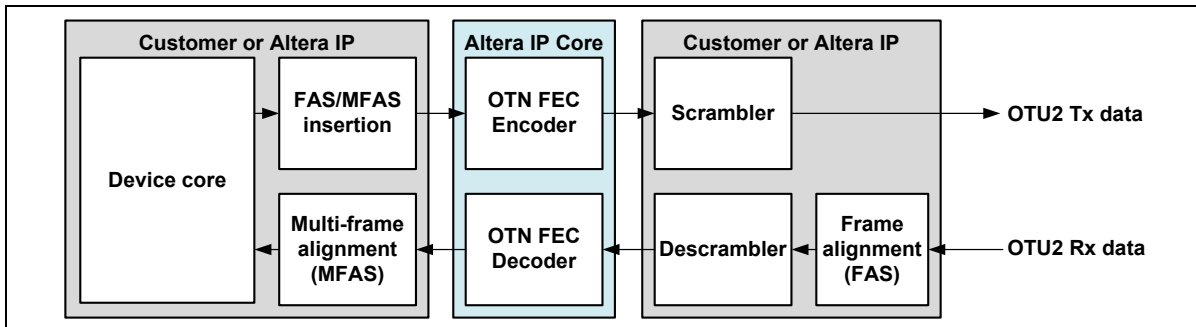


Figure 1: G.975 I.9 EFEC System Architecture

3 Performance and Resource Utilization

Arria V devices use combinational adaptive look-up tables (ALUTs) and logic registers. Table 1 shows the typical performance and resource usage for the 10 Gbit/s G.975 I.9 EFEC on a Arria V GX C3 device, commercial temperature range with speed grade 3, as reported by the Quartus® II software. The resource figures will vary slightly depending on the Quartus version used, synthesis seed numbers etc. The latencies through the encoder and decoder do not vary from frame to frame: they are a fixed number of clock cycles.

Table 1: Performance - 10 Gbit/s G.975.1 I.9 EFEC on Arria V GX

Block	ALMs	Logic Registers	Memory (M20Ks)	fMax (MHz)	Latency (Cycles)	Latency (μ s @175 MHz)
Encoder	16,873	11,533	32	>200	~8160	~48
Decoder	12,317	7,419	135	>250	~16320	~96
Top	29,109	18,952	167	>200	~24480	~144

4 Functional Overview

4.1 Encoder

The encoder expects an OTU frame including the FEC field (which will be overwritten, and the input value is thus ignored) on its input, and generates an OTU frame with the parity information added on its output.

The data to be encoded shall be delivered on `i_data` one complete frame at a time, in 2040 consecutive cycles.

The data format is MSB first, with the first bit on the line being the MSB of the word delivered to the encoder while `otn_row[1:0]` and `otn_col[8:0]` are both 0. The row number `otn_row[1:0]` ranges from 0 to 3, and the column number `otn_col[8:0]` ranges from 0 to 509. The latter is incremented every clock cycle.

The output of the encoder uses the same format, and is generated a fixed number of cycles after the input. This latency does not vary from frame to frame.

Table 2 lists the encoder input and output ports for connecting to the OTU2 G.975 I.9 EFEC IP core.

Table 2: Encoder I/O Port Listing

I/O port	Name	Port Width (Bits)	Description
in	<code>sys_clk</code>	1	Clock port.
in	<code>otn_row</code>	2	OTU2 row number; range 0-3.
in	<code>otn_col</code>	9	OTU2 column number; each column includes 8 bytes; range 0-509.
in	<code>i_data</code>	64	Data words to be encoded.
in	<code>i_bypass</code>	1	Bypass encoding.
out	<code>o_otn_row</code>	1	OTU2 row number.
out	<code>otn_col</code>	9	OTU2 column number; each column includes 8 bytes.
out	<code>o_data</code>	64	Block output.

4.2 Decoder

The decoder expects a complete I.9 OTU2 frame on its input, and from this it generates 4 OTU2 rows on its output. The output sequence mimics the way data is typically output by a GFEC decoder. E.g. 4 rows each with 3824 bytes of data and 256 bytes to discard. The block uses one clock (sys_clk) which must be OTU2/64.

The decoder output is delivered a fixed number of cycles after the input. This latency does not vary from frame to frame.

Table 3 lists the decoder input and output ports for connecting to the OTU2 G.975 I.9 EFEC IP core.

Table 3: Decoder I/O Port Listing

I/O port	Name	Port Width (Bits)	Description
in	sys_clk	1	Clock port.
in	sys_clk_rst	1	Sync reset.
in	otn_row	2	OTU2 row number.
in	otn_col	9	OTU2 column number; each column includes 8 bytes.
in	i_data	64	Data words to be decoded.
in	i_bypass	1	Bypass decoding.
in	i_scr_en	1	A value of 1 indicate that the input data is scrambled.
out	o_otn_row	1	OTU2 row number.
out	otn_col	9	OTU2 column number; each column includes 8 bytes.
out	o_data	64	Decoded output data word.
out	uncorrectable_code_errors	2	Number of BCH codes that could not be corrected in the 10 th iteration. The decoder decodes 2 codes per clock cycle, so that this output is 0, 1 or 2. It is updated in every clock cycle in the 10 th iteration.
out	correctable_code_errors	4	Number of BCH codes that is correctable in the first iteration. It is updated in very clock cycle of the first iteration.
out	ones_errors	7	Number of bits corrected 1 -> 0. Max = 64 if all the bits are corrected 1->0 in a word.
out	zeros_errors	7	Number of bits corrected 0 -> 1. Max = 64 if all the bits are corrected 0->1 in a word.

5 Synthesis constraints

5.1 Encoder

The encoder top level name is: `alt_i9_encoder` and the corresponding verilog file is named `alt_i9_encoder.sv`.

The following sections describe the settings needed to be used in a high level synthesis flow when the encoder is to be used in a larger design.

5.1.1 Parameters

DEVICE_FAMILY: Altera device family. E.g. "Arria V"

5.1.2 QSF settings

The following qsf settings are required in a higher chip level synthesis when the decoder is instantiated

```
set_global_assignment -name "REMOVE_DUPLICATE_LOGIC"           "ON"
set_global_assignment -name "REMOVE_DUPLICATE_REGISTERS"       "OFF"
set_global_assignment -name "AUTO_ROM_RECOGNITION"             "ON";
set_global_assignment -name "AUTO_RAM_RECOGNITION"             "OFF";
set_global_assignment -name "AUTO_SHIFT_REGISTER_RECOGNITION" "OFF";
```

If this conflicts with chip level preferences then these setting must be applied to the entity level instead.

5.1.3 SDC settings

The encoder entity has one clock: `sys_clk`, and these must be driven from the same PLL.

All remaining inputs and outputs to the encoder are synchronous with respect to `sys_clk` and they are all single cycle timed.

5.2 Decoder

The decoder top level name is: `alt_i9_decoder` and the corresponding verilog file is named `alt_i9_decoder.sv`.

The following sections describe the settings needed to be used in a high level synthesis flow when the decoder is to be used in a larger design.

5.2.1 Parameters

NUM_DATA_BANK: Number of banks the data RAM is split into.

NUM_CODE_PER_CYCLE: Number of BCH codes it decodes in one clock cycle.

DEVICE_FAMILY: Altera device family. E.g. "Arria V"

5.2.2 QSF settings

The following qsf settings are required in a higher chip level synthesis when the decoder is instantiated

```
set_global_assignment -name "REMOVE_DUPLICATE_LOGIC"           "ON"
set_global_assignment -name "REMOVE_DUPLICATE_REGISTERS"       "OFF"
```

```
set_global_assignment -name "AUTO_ROM_RECOGNITION" "ON";  
set_global_assignment -name "AUTO_RAM_RECOGNITION" "OFF";  
set_global_assignment -name "AUTO_SHIFT_REGISTER_RECOGNITION" "OFF";
```

If this conflicts with chip level preferences then these setting must be applied to the entity level instead.

5.2.3 SDC settings

The encoder entity has one clock: `sys_clk`, and these must be driven from the same PLL.

All remaining inputs and outputs to the encoder are synchronous with respect to `sys_clk` and they are all single cycle timed.

6 References

- [1] ITU-T Recommendation G.975.1, *Forward error correction for high bit-rate DWDM submarine systems*, ITU-T, Geneva, February 2004.

7 Revision history

Date	Revision	Description of changes
2015-02-05	0.01	<ul style="list-style-type: none">• Initial version.
2015-02-11	0.02	<ul style="list-style-type: none">• Editorial changes.