G.975 I.4 EFEC IP Core

The Altera G.975 I.4 Enhanced Forward Error Correction (G.975 I.4 EFEC) IP core demonstrates the International Telecommunication Union-Telecommunication Standardization Sector (ITU-T) G.975 standardized Reed-Solomon (RS) and Bose-Chaudhuri-Hocquenghem (BCH) super FEC algorithms. G.975 I.4 EFEC implements the standardized RS (1023, 1007) and BCH (2047, 1952) codes for Optical Transport Network (OTN) data transmission at 10 gigabits per second (Gbps)/Optical Channel Transport Unit (OTU)2 and 40 Gbps/OTU3.

Features

G.975 I.4 EFEC includes the following features:

- High-performance encoder and decoder for error detection and correction
- Data transmission available for two OTN rates:
  - 10 Gbps with 64 bit datapath width
  - 40 Gbps with 256 bit datapath width
- 7% overhead for Stratix® IV and Stratix V devices
- Latency of 107.3 µs for 10 Gbps and 24.3 µs for 40 Gbps
- Net electrical coding gain (NECG) of ~8.26 dB
- Error statistic monitoring, including the following types:
  - Corrected zeros and ones errors
  - Corrected errors and uncorrectable errors
  - 10 Gbps/OTU2 and 40 Gbps/OTU3 frame count

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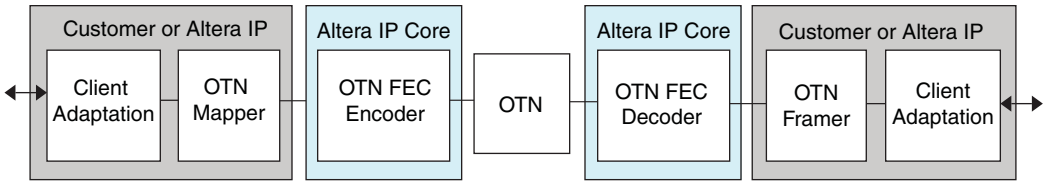
Architecture

Figure 1 illustrates the system architecture of the I.4 EFEC IP core. Data from an incoming client is adapted to OTN before it is written to the OTN mapper. The data is encoded with redundant data at the FEC encoder before it is transmitted across the network. The redundant data is decoded at the FEC decoder and identified errors are corrected before the data is written to the OTN framer. The data is then adapted back to the original client.

Figure 1. G.975 I.4 EFEC System Architecture



Device Family Support

Table 1 defines the device support levels for Altera IP cores.

Table 1. Altera IP Core Device Support Levels

FPGA Device Families	HardCopy® Device Families
Preliminary support—The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.	**HardCopy Companion**—The IP core is verified with preliminary timing models for the HardCopy companion device. The IP core meets all functional requirements, but might still be undergoing timing analysis for the HardCopy device family. It can be used in production designs with caution.
Final support—The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.	**HardCopy Compilation**—The IP core is verified with final timing models for the HardCopy device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2 lists the level of support for I.4 EFEC in each of the Altera device families.

Table 2. Device Family Support

Device Family	Support
Stratix IV GT	Final
Stratix IV E/GX	Preliminary
Stratix V E/GX/GS/GT	Preliminary
All other device families	Not available

IP Core Verification

Before releasing a version of the G.975 I.4 EFEC IP core, Altera runs comprehensive regression tests to verify its quality and correctness.

Performance and Resource Utilization

Stratix IV devices use combinational adaptive look-up tables (ALUTs) and logic registers. Table 3 shows the typical performance for 10 Gbps G.975 I.4 EFEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus® II software.

Table 3. Performance - 10 Gbps G.975 I.4 EFEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	8,794	9,558	80 blocks	2 blocks	225	~8.26 dB	107.3 µs
Decoder	46,980	44,675	114 blocks	8 blocks	254		

Table 4 shows the typical performance for 40 Gbps G.975 I.4 EFEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus II software.

Table 4. Performance - 40 Gbps G.975 I.4 EFEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	18,269	15,358	176 blocks	0 blocks	202	8.26 dB	24.3 µs
Decoder	107,587	85,617	214 blocks	0 blocks	205		

Port Listing

Table 5 lists the encoder input and output ports for connecting to the G.975 I.4 EFEC IP core.

Table 5. Encoder I/O Port Listing (Part 1 of 2)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Input	sys_clk	1	1	Clock port.
Input	rst	1	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	rs_enable_n	1	1	Enable the RS encoder. This is a synchronous signal and is active low.
Input	bch_enable_n	1	1	Enables the BCH encoder port. This is a synchronous signal and is active low.
Input	otn_row	2	2	Input OTN frame row port. This is a synchronous signal.
Input	otn_col	9	7	Input OTN frame column port. This is a synchronous signal.
Input	data_in	64	256	Input enable data port. This is a synchronous signal and is active high.
Output	otn_row_out	2	2	Output OTN frame row port. This is a synchronous signal.

Table 5. Encoder I/O Port Listing (Part 2 of 2)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Output	otn_col_out	9	7	Output OTN frame column port. This is a synchronous signal.
Output	data_out	64	256	Output data port.

Table 6 lists the decoder input and output ports for connecting to the G.975 I.4 EFEC IP core. All error counts are accumulated on a per-clock cycle basis.

Table 6. Decoder I/O Port Listing (Part 1 of 4)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Input	sys_clk	1	1	Clock port.
Input	rst	1	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	rs1_enable_n	1	1	Enables the first RS decoder. This is a synchronous signal and is active low.
Input	rs2_enable_n	1	1	Enables the second RS decoder. This is a synchronous signal and is active low.
Input	bch1_enable_n	1	1	Enables the first BCH decoder. This is a synchronous signal and is active low.
Input	bch2_enable_n	1	1	Enables the second BCH decoder port. This is a synchronous signal and is active low.
Input	rs1_error_scrambler_en_n	1	1	This input enables the first RS decoder's error scrambling. This is a synchronous signal and is active low.
Input	rs2_error_scrambler_en_n	1	1	This input enables the second RS decoder's error scrambling. This is a synchronous signal and is active low.
Input	bch1_error_scrambler_en_n	1	1	This input enables the first BCH decoder's error scrambling. This is a synchronous signal and is active low.
Input	bch2_error_scrambler_en_n	1	1	This input enables the second BCH decoder's error scrambling. This is a synchronous signal and is active low.
Input	otn_row	2	2	Input OTN frame row port. This is a synchronous signal.
Input	otn_col	9	7	Input OTN frame column port. This is a synchronous signal.
Input	data_in	64	256	Input data port.
Output	otn_row_out	2	2	Output OTN frame row port. This is a synchronous signal.

Table 6. Decoder I/O Port Listing (Part 2 of 4)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Output	otn_col_out	9	7	Output OTN frame column port. This is a synchronous signal.
Output	rs1_uncorrectable_code_ errors_valid	1	1	This output is the valid signal for rs1_uncorrectable_code_ errors. This is a synchronous signal and is active high.
Output	rs2_uncorrectable_code_ errors_valid	1	1	This output is the valid signal for rs2_uncorrectable_code_ errors. This is a synchronous signal and is active high.
Output	bch1_uncorrectable_code_ errors_valid	1	1	This output is the valid signal for bch1_uncorrectable_code_ errors. This is a synchronous signal and is active high.
Output	bch2_uncorrectable_code_ errors_valid	1	1	This output is the valid signal for bch2_uncorrectable_code_ errors. This is a synchronous signal and is active high.
Output	rs1_correctable_code_ errors_valid	1	1	This output is the valid signal for rs1_correctable_code_ errors. This is a synchronous signal and is active high.
Output	rs2_correctable_code_ errors_valid	1	1	This output is the valid signal for rs2_correctable_code_ errors. This is a synchronous signal and is active high.
Output	bch1_correctable_code_ errors_valid	1	1	This output is the valid signal for bch1_correctable_code_ errors. This is a synchronous signal and is active high.
Output	bch2_correctable_code_ errors_valid	1	1	This output is the valid signal for bch2_correctable_code_ errors. This is a synchronous signal and is active high.
Output	rs1_ones_errors_valid	1	1	This output is the valid signal for rs1_ones_errors. This is a synchronous signal and is active high.
Output	rs2_ones_errors_valid	1	1	This output is the valid signal for rs2_ones_errors. This is a synchronous signal and is active high.
Output	rs1_zeros_errors_valid	1	1	This output is the valid signal for rs1_zeros_errors. This is a synchronous signal and is active high.
Output	rs2_zeros_errors_valid	1	1	This output is the valid signal for rs2_zeros_errors. This is a synchronous signal and is active high.

Table 6. Decoder I/O Port Listing (Part 3 of 4)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Output	rs1_ones_errors	7	9	This output signals the number of ones errors corrected by the first RS decoder.
Output	rs1_zeros_errors	7	9	This output signals the number of zeros errors corrected by the first RS decoder.
Output	rs2_ones_errors	7	9	This output signals the number of ones errors corrected by the second RS decoder.
Output	rs2_zeros_errors	7	9	This output signals the number of zeros errors corrected by the second RS decoder.
Output	bch1_ones_errors	7	9	This output signals the number of ones errors corrected by the first BCH decoder.
Output	bch1_zeros_errors	7	9	This output signals the number of zeros errors corrected by the first BCH decoder.
Output	bch2_ones_errors	7	9	This output signals the number of ones errors corrected by the second BCH decoder.
Output	bch2_zeros_errors	7	9	This output signals the number of zeros errors corrected by the second BCH decoder.
Output	rs1_uncorrectable_code_ errors	1	1	This output signals the number of uncorrectable codes from the first RS decoder. This is a synchronous signal and is active high.
Output	rs1_correctable_code_ errors	1	1	This output signals the number of correctable codes from the first RS decoder. This is a synchronous signal and is active high.
Output	rs2_uncorrectable_code_ errors	1	1	This output signals the number of uncorrectable codes from the second RS decoder. This is a synchronous signal and is active high.
Output	rs2_correctable_code_ errors	1	1	This output signals the number of correctable codes from the second RS decoder. This is a synchronous signal and is active high.
Output	bch1_uncorrectable_code_errors	1	2	This output signals the number of uncorrectable codes from the first BCH decoder. This is a synchronous signal and is active high.
Output	bch1_correctable_code_ errors	1	2	This output signals the number of correctable codes from the first BCH decoder. This is a synchronous signal and is active high.

Table 6. Decoder I/O Port Listing (Part 4 of 4)

I/O	Port	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Output	bch2_uncorrectable_code_ errors	1	2	This output signals the number of uncorrectable codes from the second BCH decoder. This is a synchronous signal and is active high.
Output	bch2_correctable_code_ errors	1	2	This output signals the number of correctable codes from the second BCH decoder. This is a synchronous signal and is active high.
Output	data_out	64	256	Output data port.

Additional Information

Recommendation G.975: Forward Error Correction for High Bit-Rate DWDM Submarine Systems available on the ITU website (www.itu.int) has complete details on G.975 I.4 FEC.

Document Revision History

Table 7 shows the revision history for this document.

Table 7. Document Revision History

Date	Version	Changes
February 2012	1.0	Initial release.