G.709 FEC IP Core

The Altera G.709 Forward Error Correction (G.709 FEC) IP core demonstrates the International Telecommunication Union-Telecommunication Standardization Sector (ITU-T) G.709 application of the Reed-Solomon (RS) algorithm in Optical Transport Network (OTN) data transmission. G.709 FEC implements the standardized RS (255, 239) code for transmission at 2.5 gigabits per second (Gbps)/Optical Channel Transport Unit (OTU)1, 10 Gbps/OTU2, 40 Gbps/OTU3, and 100 Gbps/OTU4.

Features

G.709 FEC includes the following features:

- High-performance encoder and decoder for error detection and correction
- Data transmission available for four OTN rates:
  - 2.5 Gbps/OTU1 with 16 bit datapath width
  - 10 Gbps/OTU2 with 64 bit datapath width
  - 40 Gbps/OTU3 with 256 bit datapath width
  - 100 Gbps/OTU4 with 640 bit datapath width
- 7% overhead for Stratix® IV and Stratix V devices
- Net electrical coding gain (NECG) of 6.5 dB
- Error statistic monitoring, including the following types:
  - Corrected zeros and ones errors
  - Corrected errors and uncorrectable errors
  - 2.5 Gbps/OTU1, 10 Gbps/OTU2, 40 Gbps/OTU3, or 100 Gbps/OTU4 frame count

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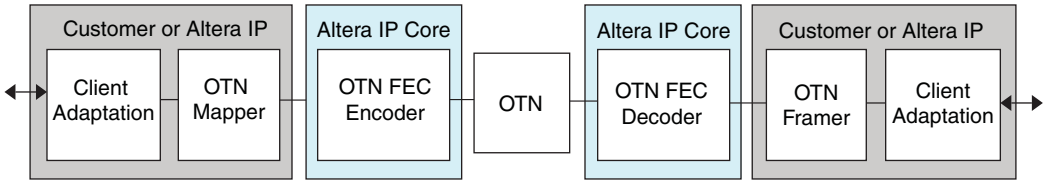
Architecture

Figure 1 illustrates the system architecture of the G.709 FEC IP core. Data from an incoming client is adapted to OTN before it is written to the OTN mapper. The data is encoded with redundant data at the FEC encoder before it is transmitted across the network. The redundant data is decoded at the FEC decoder and identified errors are corrected before the data is written to the OTN framer. The data is then adapted back to the original client.

Figure 1. G.709 FEC System Architecture



Device Family Support

Table 1 defines the device support levels for Altera IP cores.

Table 1. Altera IP Core Device Support Levels

FPGA Device Families	HardCopy® Device Families
Preliminary support—The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.	**HardCopy Companion**—The IP core is verified with preliminary timing models for the HardCopy companion device. The IP core meets all functional requirements, but might still be undergoing timing analysis for the HardCopy device family. It can be used in production designs with caution.
Final support—The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.	**HardCopy Compilation**—The IP core is verified with final timing models for the HardCopy device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2 lists the level of support for 2.5 Gbps G.709 FEC in each of the Altera device families.

Table 2. Device Family Support

Device Family	Support
Stratix IV GX/GT	Final
Stratix IV E	Preliminary
Stratix V E/GX/GS/GT	Preliminary
All other device families	Not available

Table 3 lists the level of support for 10 Gbps, 40 Gbps, and 100 Gbps G.709 FEC in each of the Altera device families.

Table 3. Device Family Support

Device Family	Support
Stratix IV GT	Final
Stratix IV E/GX	Preliminary
Stratix V E/GX/GS/GT	Preliminary
All other device families	Not available

IP Core Verification

Before releasing a version of the G.709 FEC IP core, Altera runs comprehensive regression tests to verify its quality and correctness.

Performance and Resource Utilization

The OTN frame consists of 4080 data bytes with 4 rows of information. The rate of data transmission determines the number of columns and datapath width for various speeds. G.709 FEC frame information is outlined in Table 4.

Table 4. G.709 FEC Framing Information

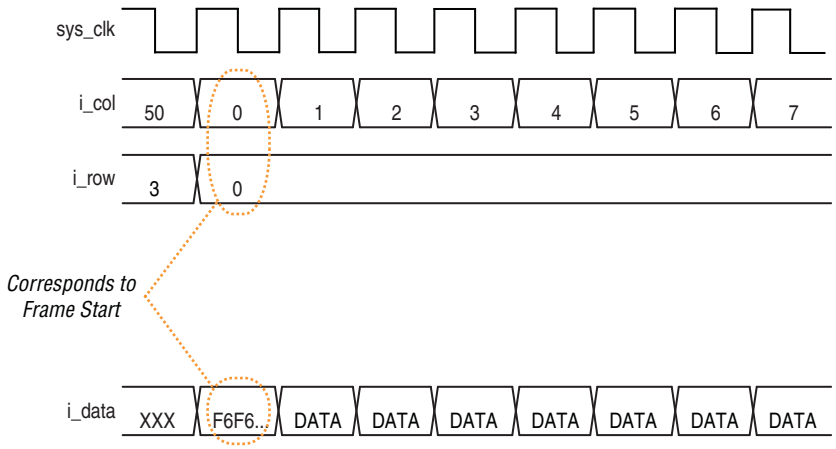
	2.5 Gbps G.709 FEC	10 Gbps G.709 FEC	40 Gbps G.709 FEC	100 Gbps G.709 FEC
Number of Columns	2040	510	126/127	51
Number of Rows	4	4	4	4
Datapath Width	2 bytes	8 bytes	32 bytes	80 bytes

Note to Table 4:

(1) The number of columns in the 40 Gbps OTN frame alternates between 126 and 127.

Figure 2 illustrates the input timing information for G.709 FEC at 100 Gbps. As shown, the IP core provides synchronous timing with the OTN column (`i_col`) and row (`i_row`) occurring with the positive edge of the system clock (`sys_clk`) and corresponding with the start of the OTN frame (denoted as F6F6... in the `i_data` port).

Figure 2. Example 100 Gbps G.709 FEC Input Timing Diagram



Stratix IV devices use combinational adaptive look-up tables (ALUTs) and logic registers. Table 5 shows the typical performance for 2.5 Gbps G.709 FEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus® II software.

Table 5. Performance - 2.5 Gbps G.709 FEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	297	2,178	0 blocks	0 blocks	383.73	6.5 dB	6.3 µs
Decoder	5,168	10,396	8 blocks	0 blocks	207.51		

Table 6 shows the typical performance for 10 Gbps G.709 FEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus II software.

Table 6. Performance - 10 Gbps G.709 FEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	1,153	2,358	0 blocks	0 blocks	297.18	6.5 dB	6.3 µs
Decoder	7,872	12,206	8 blocks	0 blocks	226.55		

Table 7 shows the typical performance for 40 Gbps G.709 FEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus II software.

Table 7. Performance - 40 Gbps G.709 FEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	3,500	3,127	0 blocks	0 blocks	212.53	6.5 dB	6 µs
Decoder	25,000	23,155	17 blocks	0 blocks	204.92		

Table 8 shows the typical performance for 100 Gbps G.709 FEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus II software.

Table 8. Performance - 100 Gbps G.709 FEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	8,500	5,556	0 blocks	0 blocks	242.51	6.5 dB	< 1 µs
Decoder	44,000	44,415	22 blocks	0 blocks	220.9		

The nominal latency for the 100 Gbps G.709 FEC encoder is 5 clock cycles and the decoder is 161 clock cycles. The nominal latency is produced by continuously asserting the `i_data_en` port on the encoder and decoder; this allows the core to run at the full rate.

Port Listing

Table 9 lists the encoder input and output ports for connecting to the 2.5 Gbps, 10 Gbps, and 40 Gbps G.709 FEC IP cores.

Table 9. Encoder I/O Port Listing for 2.5 Gbps, 10 Gbps, and 40 Gbps G.709 FECs

I/O	Port	2.5 Gbps Port Width (Bits)	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Input	`sys_clk`	1	1	1	Clock port.
Input	`i_enable_n`	1	1	1	Input enable encoder and decoder port. This is a synchronous signal and is active low.
Input	`i_row`	2	2	2	Input OTN frame row port. This is a synchronous signal.
Input	`i_col`	11	9	7	Input OTN frame column port. This is a synchronous signal.
Input	`i_data`	16	64	256	Input data port.
Output	`o_row`	2	2	2	Output OTN frame row port. This is a synchronous signal.
Output	`o_col`	11	9	7	Output OTN frame column port. This is a synchronous signal.
Output	`o_data`	16	64	256	Output data port.

Table 10 lists in the decoder input and output ports for connecting to the 2.5 Gbps 10 Gbps, and 40 Gbps G.709 FEC IP cores.

Table 10. Decoder I/O Port Listing for 2.5 Gbps, 10 Gbps, and 40 Gbps G.709 FECs (Part 1 of 2)

I/O	Port	2.5 Gbps Port Width (Bits)	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Input	sys_clk	1	1	1	Clock port.
Input	rst	1	1	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	enable_n	1	1	1	Enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_error_scrambler_en_n	1	1	1	This input enables error scrambling. This is a synchronous signal and is active low.
Input	i_row	2	2	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	11	9	7	Input OTN frame column port. This is a synchronous signal.
Input	data_in	16	64	256	Input data port.
Output	o_uncorrectable_code_errors_valid	1	1	1	This output is the valid signal for o_uncorrectable_code_errors_inst. This is a synchronous signal and is active high.
Output	uncorrectable_code_errors	1	1	2	This output signals the number of uncorrectable RS codes. This is a synchronous signal and is active high.
Output	o_correctable_code_errors_valid	1	1	1	This output is the valid signal for o_correctable_code_errors_inst. This is a synchronous signal and is active high.
Output	correctable_code_errors	1	1	2	This output signals the number of correctable RS codes. This is a synchronous signal and is active high.
Output	o_correctable_block_errors_valid	1	1	1	This output is the valid signal for o_correctable_block_errors_inst. This is a synchronous signal and is active high.
Output	correctable_block_errors	4	4	5	This output signals the number of correctable RS block errors. This is a synchronous signal and is active high.
Output	ones_errors	9	7	9	This output signals the number of corrected ones errors.
Output	zeros_errors	9	7	9	This output signals the number of corrected zeros errors.
Output	o_row	2	2	2	Output OTN frame row port. This is a synchronous signal.

Table 10. Decoder I/O Port Listing for 2.5 Gbps, 10 Gbps, and 40 Gbps G.709 FECs (Part 2 of 2)

I/O	Port	2.5 Gbps Port Width (Bits)	10 Gbps Port Width (Bits)	40 Gbps Port Width (Bits)	Description
Output	o_col	11	9	7	Output OTN frame column port. This is a synchronous signal.
Output	o_data	16	64	256	Output data port.

Table 11 lists the encoder input and output ports for connecting to the 100 Gbps G.709 FEC IP core.

Table 11. Encoder I/O Port Listing for 100 Gbps G.709 FEC

I/O	Port	100 Gbps Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	i_enable_n	1	Input enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	6	Input OTN frame column port. This is a synchronous signal.
Input	i_data_en	1	Input enable data port. This is a synchronous signal and is active high.
Input	i_data	640	Input data port.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	6	Output OTN frame column port. This is a synchronous signal.
Output	o_data_en	1	Ouput enable data port. This is a synchronous signal and is active high.
Output	o_data	640	Output data port.

Table 12 lists in the decoder input and output ports for connecting to the 100 Gbps G.709 FEC IP core.

Table 12. Decoder I/O Port Listing for 100 Gbps G.709 FEC (Part 1 of 3)

I/O	Port	100 Gbps Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	rst	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	enable_n	1	Enable encoder and decoder port. This is a synchronous signal and is active low.

Table 12. Decoder I/O Port Listing for 100 Gbps G.709 FEC (Part 2 of 3)

I/O	Port	100 Gbps Port Width (Bits)	Description
Input	i_error_scrambler_en_n	1	This input enables error scrambling. This is a synchronous signal and is active low.
Input	i_disable_data_correction	1	This input disables data correction while providing full monitoring capabilities. This is a synchronous signal and is active high.
Input	i_count_suppression	1	This input suppresses error count statistics. This is a synchronous signal and is active high.
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	6	Input OTN frame column port. This is a synchronous signal.
Input	i_data_en	1	Input enable data port. This is a synchronous signal and is active high.
Input	i_data	640	Input data port.
Input	i_latch_counters	1	This input sets the interval used by the accumulation counters. The signal is a positive-edge triggered latch; when a positive edge is received, the output value of the accumulation counters is updated with the error count of the previous interval and the internal accumulation count is reset. The i_latch_counters and sys_clk signals must be synchronous to the same clock domain.
Output	o_0s_fec_errors	32	This output signals the number of zeros errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_1s_fec_errors	32	This output signals the number of ones errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_fec_errors	32	This output signals the total number of errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_uncorrectables	32	This output signals the number of uncorrectable RS codes. It is controlled by i_latch_counters.
Output	o_correctable_blocks	32	This output signals the number of correctable RS block errors It is controlled by i_latch_counters.
Output	o_otu4_frames	32	Output OTU4 frames port. This is a synchronous signal. It is controlled by i_latch_counters.
Output	o_uncorrectable_code_errors_valid	1	This output is the valid signal for o_uncorrectable_code_errors_inst. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.
Output	o_uncorrectable_code_errors_inst	3	This output signals the number of uncorrectable RS codes. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.

Table 12. Decoder I/O Port Listing for 100 Gbps G.709 FEC (Part 3 of 3)

I/O	Port	100 Gbps Port Width (Bits)	Description
Output	o_correctable_code_errors_valid	1	This output is the valid signal for o_correctable_code_errors_inst. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.
Output	o_correctable_code_errors_inst	3	This output signals the number of correctable RS codes. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.
Output	o_correctable_block_errors_valid	1	This output is the valid signal for o_correctable_block_errors_inst. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.
Output	o_correctable_block_errors_inst	6	This output signals the number of correctable RS block errors. The value is accumulated on a per-clock cycle basis. This is a synchronous signal and is active high.
Output	o_ones_zeros_errors_valid	1	This output is the valid signal for o_ones_errors_inst and o_zeros_errors_inst. The value is accumulated on a per-clock cycle basis.
Output	o_ones_errors_inst	10	This output signals the number of corrected ones errors. The value is accumulated on a per-clock cycle basis.
Output	o_zeros_errors_inst	10	This output signals the number of corrected zeros errors. The value is accumulated on a per-clock cycle basis.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	6	Output OTN frame column port. This is a synchronous signal.
Output	o_data_en	1	Output enable data port. This is a synchronous signal and is active high.
Output	o_data	640	Output data port.

Additional Information

Recommendation *G.709: Interfaces for the Optical Transport Network (OTN)* available on the ITU website (www.itu.int) has complete details on G.709 FEC.

Document Revision History

Table 13 shows the revision history for this document.

Table 13. Document Revision History

Date	Version	Changes
February 2012	1.0	Initial release.