Pin Information for the Stratix® IV GX EP4SGX70 Device
Version 1.4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1A		TDI		TDI			J20	No			
1A		TMS		TMS			G23	No			
1A		TRST		TRST			D26	No			
1A		TCK		TCK			D25	No			
1A		TDO		TDO			E25	No			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	H23	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	H22	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	D28	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G24	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C28	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	F26	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	F25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	E28	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E27	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H25	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	H24	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	G27	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	G26	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K24	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K23	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	F28	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G28	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K22	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K21	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L21	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L20	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	H27	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	K26	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K25	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	L24	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M23	Yes			
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	Yes	DQSn5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	Yes	DQS5L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	N21	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	N20	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	J28	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	K28	Yes	DQ5L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N23	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	N22	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	L28	Yes	DQSn6L	DQ5L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	K27	Yes	DQS6L	DQ5L/CQn5L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	P21	Yes	DQ6L	DQ5L	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	P20	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	M26	Yes	DQSn7L	DQSn5L/DQ5L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	M25	Yes	DQS7L	DQS5L/CQ5L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N25	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	N24	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	M28	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	L27	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P26	No			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P25	No			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N28	No			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N27	No			
1C	VREFB1CN0	CLK1n	CLK1n				P28	No			
1C	VREFB1CN0	CLK1p	CLK1p				P27	No			
2C	VREFB2CN0	CLK3p	CLK3p				T28	No			
2C	VREFB2CN0	CLK3n	CLK3n				R28	No			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	T27	No			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	U28	No			
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R25	No			
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R26	No			
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	T25	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	U26	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	R20	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	T21	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	U27	Yes	DQS8L	DQS10L/CQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	Yes	DQSn8L	DQSn10L/DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T22	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T23	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	U25	Yes	DQS9L	DQ10L/CQn10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	V26	Yes	DQSn9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T20	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U21	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	U23	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	U24	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V25	Yes	DQS10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	W26	Yes	DQSn10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V22	Yes			
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	V23	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L21p	DIFFOUT_L41p	Y27	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L21n	DIFFOUT_L41n	Y28	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L21p	DIFFOUT_L42p	W24	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L21n	DIFFOUT_L42n	W25	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L22p	DIFFOUT_L43p	AB28	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L22n	DIFFOUT_L43n	AA28	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22p	DIFFOUT_L44p	W22	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22n	DIFFOUT_L44n	W23	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	AB27	Yes	DQS11L	DQS13L/CQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	AC28	Yes	DQSn11L	DQSn13L/DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	Yes	DQ12L	DQ13L	DQ14L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	W21	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC27	Yes	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AD28	Yes	DQSn12L	DQ13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	Y25	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	Y26	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AA25	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AA26	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB25	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AE27	Yes	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AE28	Yes	DQSn13L	DQSn14L/DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	Y23	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	Y24	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AF27	Yes	DQS14L	DQ14L/CQn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	Yes	DQSn14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AB23	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AB24	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AH27	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AG28	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AC25	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD26	Yes			
		nCONFIG		nCONFIG			AA22	No			
		nSTATUS		nSTATUS			AC23	No			
		CONF_DONE		CONF_DONE			AC24	No			
		PORSEL					W20	No			
		nCE		nCE			Y21	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AB21	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AC21	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AD22	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AC22	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AA20	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AB20	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE23	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD23	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AE24	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AE25	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AG23	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AF24	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AF25	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF26	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH25	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG25	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AG26	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AH26	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AG22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AF22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AE22	Yes	DQ4B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
3A	VREFB3AN0	IO				DIFFOUT_B13n	AH20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AH21	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AG19	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AG20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AF19	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AE20	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AD19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AC19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD20	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AA19	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AB18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17	Yes			
3C	VREFB3CN0	IO				DIFFOUT_B21n	AA17	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B21p	AA16	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AC18	Yes	DQSn7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AB17	Yes	DQS7B	DQ7B/CQn7B	
3C	VREFB3CN0	IO				DIFFOUT_B23n	Y15	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B23p	Y16	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AH19	Yes	DQSn8B	DQSn7B/DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AH18	Yes	DQS8B	DQS7B/CQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE17	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25p	AG17	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF18	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE18	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AD17	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AD16	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AF16	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AE16	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AC16	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	AB15	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AF15	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AE15	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH17	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AG16	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AH16	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AH15	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AG14	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AH14	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AH12	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH13	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AF14	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AG13	Yes			
4C	VREFB4CN0	IO				DIFFOUT_B36p	Y13	Yes	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B36n	Y14	Yes	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AA13	Yes	DQS9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AA14	Yes	DQSn9B		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
4C	VREFB4CN0	IO				DIFFOUT_B38p	AB12	Yes	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B38n	AB11	Yes	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AD13	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AE12	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40p	AE13	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40n	AE14	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AC12	Yes	DQS10B	DQS11B/CQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AD11	Yes	DQSn10B	DQSn11B/DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42p	AF12	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42n	AH11	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AE11	Yes	DQS11B	DQ11B/CQn11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AF11	Yes	DQSn11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44p	AH10	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44n	AG11	Yes	DQ11B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	Y12	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	AA11	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B46p	Y10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B46n	Y11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AC10	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AD10	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48p	AB9	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48n	AB10	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9	Yes	DQS12B	DQS15B/CQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AE10	Yes	DQSn12B	DQSn15B/DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50p	AF10	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50n	AF9	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG8	Yes	DQS13B	DQ15B/CQn15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH8	Yes	DQSn13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52p	AH9	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52n	AG10	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AG7	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AH6	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54p	AH5	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54n	AH7	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AF6	Yes	DQS14B	DQS16B/CQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AG5	Yes	DQSn14B	DQSn16B/DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56p	AE7	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56n	AE8	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AE6	Yes	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AF7	Yes	DQSn15B	DQ16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58p	AD7	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58n	AD8	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AG4	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AH4	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AF3	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AF4	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AH2	Yes	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AH3	Yes	DQSn16B	DQSn17B/DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AC6	Yes	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AC8	Yes	DQ17B	DQ17B	DQ17B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AA8	Yes	DQS17B	DQ17B/CQn17B	DQ17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AB7	Yes	DQSn17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	Y9	Yes	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AA10	Yes	DQ17B	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			Y8	No			
		nCEO		nCEO			W6	No			
		DCLK		DCLK			Y6	No			
		nCSO		nCSO			W7	No			
		ASDO		ASDO			Y7	No			
		MSEL2		MSEL2			J7	No			
		MSEL1		MSEL1			J9	No			
		MSEL0		MSEL0			K9	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	F7	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	G8	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F8	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	G9	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	H9	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D6	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E6	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	D5	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	F6	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	C4	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	A2	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	B3	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	A3	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	B4	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	A5	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	A4	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A6	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B6	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	C7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	D7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	A9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	D10	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	E9	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	F10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	E10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	C10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	D9	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	H10	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	G11	Yes			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12	Yes			
7C	VREFB7CN0	IO				DIFFOUT_T21n	A11	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T21p	A10	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	C11	Yes	DQSn7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	D11	Yes	DQS7T	DQ7T/CQn7T	
7C	VREFB7CN0	IO				DIFFOUT_T23n	B12	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T23p	D12	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	E12	Yes	DQSn8T	DQSn7T/DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	F11	Yes	DQS8T	DQS7T/CQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25n	F13	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25p	E13	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D13	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T27n	H12	Yes	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T27p	G12	Yes	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	G14	Yes	DQSn9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	H13	Yes	DQS9T		
7C	VREFB7CN0	IO				DIFFOUT_T29n	J14	Yes	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T29p	J13	Yes	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C14	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D14	Yes			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A14	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B13	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A12	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	A13	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	B15	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A15	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B16	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A16	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	D15	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	C15	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J15	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	H15	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	J16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	A19	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A18	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40p	A17	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40n	B18	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C18	Yes	DQS10T	DQS11T/CQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C17	Yes	DQSn10T	DQSn11T/DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42p	G17	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42n	D17	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	F17	Yes	DQS11T	DQ11T/CQn11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	E18	Yes	DQSn11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44p	D18	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	Yes	DQ11T	DQ11T	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	J17	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	H18	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T46p	H19	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T46n	J18	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	C19	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	B19	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48p	A20	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48n	A21	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	C20	Yes	DQS12T	DQS15T/CQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	B21	Yes	DQSn12T	DQSn15T/DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50p	F19	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50n	G19	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	E19	Yes	DQS13T	DQ15T/CQn15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	D19	Yes	DQSn13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52p	D20	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52n	F20	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D21	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C21	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54p	A22	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54n	A23	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	C22	Yes	DQS14T	DQS16T/CQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	B22	Yes	DQSn14T	DQSn16T/DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56p	H21	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56n	E21	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	E22	Yes	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	D22	Yes	DQSn15T	DQ16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58p	G21	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58n	F21	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B24	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A24	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	D24	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	C25	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D23	Yes	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24	Yes	DQSn16T	DQSn17T/DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	A26	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	C26	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	B25	Yes	DQS17T	DQ17T/CQn17T	DQ17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	A25	Yes	DQSn17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	A27	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	B27	Yes	DQ17T	DQ17T	DQ17T
QR0		GXB_RX_R0p					AD2	No			
QR0		GXB_RX_R0n					AD1	No			
QR0		GXB_TX_R0p					AC4	No			
QR0		GXB_TX_R0n					AC3	No			
QR0		GXB_RX_R1p					AB2	No			
QR0		GXB_RX_R1n					AB1	No			
QR0		GXB_TX_R1p					AA4	No			
QR0		GXB_TX_R1n					AA3	No			
QR0		REFCLK_R0p,GXB_CMURX_R0p					Y2	No			
QR0		REFCLK_R0n,GXB_CMURX_R0n					Y1	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
QR0		REFCLK_R1p,GXB_CMURX_R1p					W4	No			
QR0		REFCLK_R1n,GXB_CMURX_R1n					W3	No			
QR0		GXB_RX_R2p					V2	No			
QR0		GXB_RX_R2n					V1	No			
QR0		GXB_TX_R2p					U4	No			
QR0		GXB_TX_R2n					U3	No			
QR0		GXB_RX_R3p					T2	No			
QR0		GXB_RX_R3n					T1	No			
QR0		GXB_TX_R3p					R4	No			
QR0		GXB_TX_R3n					R3	No			
QR1		GXB_RX_R4p					P2	No			
QR1		GXB_RX_R4n					P1	No			
QR1		GXB_TX_R4p					N4	No			
QR1		GXB_TX_R4n					N3	No			
QR1		GXB_RX_R5p					M2	No			
QR1		GXB_RX_R5n					M1	No			
QR1		GXB_TX_R5p					L4	No			
QR1		GXB_TX_R5n					L3	No			
QR1		REFCLK_R2p,GXB_CMURX_R2p					K2	No			
QR1		REFCLK_R2n,GXB_CMURX_R2n					K1	No			
QR1		REFCLK_R3p,GXB_CMURX_R3p					J4	No			
QR1		REFCLK_R3n,GXB_CMURX_R3n					J3	No			
QR1		GXB_RX_R6p					H2	No			
QR1		GXB_RX_R6n					H1	No			
QR1		GXB_TX_R6p					G4	No			
QR1		GXB_TX_R6n					G3	No			
QR1		GXB_RX_R7p					F2	No			
QR1		GXB_RX_R7n					F1	No			
QR1		GXB_TX_R7p					E4	No			
QR1		GXB_TX_R7n					E3	No			
		GND					W8	No			
		GND					P15	No			
		GND					AG3	No			
		GND					AG6	No			
		GND					AG9	No			
		GND					AG12	No			
		GND					AG15	No			
		GND					AG18	No			
		GND					AG21	No			
		GND					AG24	No			
		GND					AG27	No			
		GND					AD6	No			
		GND					AD9	No			
		GND					AD12	No			
		GND					AD15	No			
		GND					AD18	No			
		GND					AD21	No			
		GND					AD24	No			
		GND					AD27	No			
		GND					AA6	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					AA9	No			
		GND					AA12	No			
		GND					AA15	No			
		GND					AA18	No			
		GND					AA21	No			
		GND					AA24	No			
		GND					AA27	No			
		GND					W12	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					W19	No			
		GND					V9	No			
		GND					V11	No			
		GND					V13	No			
		GND					V15	No			
		GND					V17	No			
		GND					V19	No			
		GND					V21	No			
		GND					V24	No			
		GND					V27	No			
		GND					U12	No			
		GND					U14	No			
		GND					U16	No			
		GND					U18	No			
		GND					T11	No			
		GND					T13	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					R12	No			
		GND					R16	No			
		GND					R18	No			
		GND					R21	No			
		GND					R24	No			
		GND					R27	No			
		GND					P11	No			
		GND					P13	No			
		GND					P17	No			
		GND					P19	No			
		GND					N12	No			
		GND					N14	No			
		GND					N16	No			
		GND					N18	No			
		GND					M11	No			
		GND					M13	No			
		GND					M15	No			
		GND					M17	No			
		GND					M19	No			
		GND					M21	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					M24	No			
		GND					M27	No			
		GND					L8	No			
		GND					L12	No			
		GND					L14	No			
		GND					L16	No			
		GND					L18	No			
		GND					K11	No			
		GND					K13	No			
		GND					K15	No			
		GND					K17	No			
		GND					K19	No			
		GND					J21	No			
		GND					J24	No			
		GND					J27	No			
		GND					H5	No			
		GND					H8	No			
		GND					H11	No			
		GND					H14	No			
		GND					H17	No			
		GND					H20	No			
		GND					F24	No			
		GND					F27	No			
		GND					E5	No			
		GND					E8	No			
		GND					E11	No			
		GND					E14	No			
		GND					E17	No			
		GND					E20	No			
		GND					E23	No			
		GND					C27	No			
		GND					B2	No			
		GND					B5	No			
		GND					B8	No			
		GND					B11	No			
		GND					B14	No			
		GND					B17	No			
		GND					B20	No			
		GND					B23	No			
		GND					B26	No			
		GND					C2	No			
		GND					C1	No			
		GND					D4	No			
		GND					D3	No			
		GND					D2	No			
		GND					E2	No			
		GND					E1	No			
		GND					F4	No			
		GND					F3	No			
		GND					G2	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					G1	No			
		GND					H4	No			
		GND					H3	No			
		GND					J2	No			
		GND					J1	No			
		GND					K4	No			
		GND					K3	No			
		GND					L5	No			
		GND					L2	No			
		GND					L1	No			
		GND					M6	No			
		GND					M4	No			
		GND					M3	No			
		GND					N7	No			
		GND					N5	No			
		GND					N2	No			
		GND					N1	No			
		GND					P8	No			
		GND					P6	No			
		GND					P4	No			
		GND					P3	No			
		GND					R7	No			
		GND					R5	No			
		GND					R2	No			
		GND					R1	No			
		GND					T8	No			
		GND					T6	No			
		GND					T4	No			
		GND					T3	No			
		GND					U5	No			
		GND					U2	No			
		GND					U1	No			
		GND					V6	No			
		GND					V4	No			
		GND					V3	No			
		GND					W2	No			
		GND					W1	No			
		GND					Y4	No			
		GND					Y3	No			
		GND					AA2	No			
		GND					AA1	No			
		GND					AB4	No			
		GND					AB3	No			
		GND					AC2	No			
		GND					AC1	No			
		GND					AD4	No			
		GND					AD3	No			
		GND					AE2	No			
		GND					AE1	No			
		GND					AF2	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					AG2	No			
		GND					AG1	No			
		VCC					P14	No			
		VCC					V14	No			
		VCC					V18	No			
		VCC					U11	No			
		VCC					U13	No			
		VCC					U15	No			
		VCC					U17	No			
		VCC					T12	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					R13	No			
		VCC					R15	No			
		VCC					R17	No			
		VCC					P12	No			
		VCC					P16	No			
		VCC					N13	No			
		VCC					N15	No			
		VCC					N17	No			
		VCC					M12	No			
		VCC					M14	No			
		VCC					M16	No			
		VCC					P18	No			
		VCC					L11	No			
		VCC					L17	No			
		VCC					L13	No			
		VCC					L15	No			
		VCC					N11	No			
		VCC					M18	No			
		VCC					R11	No			
		VCC					T18	No			
		VCC					V12	No			
		VCC					V16	No			
		VCC					U7	No			
		VCC					U8	No			
		VCC					M7	No			
		VCC					M8	No			
		VCCPT					R22	No			
		VCCPT					P22	No			
		VCCPT					AB14	No			
		VCCPT					R10	No			
		VCCPT					P10	No			
		VCCPT					G15	No			
		DNU					R14	No			
		VCCPGM					Y20	No			
		VCCPGM					W9	No			
		TEMPDIODEn					H7	No			
		TEMPDIODEp					G6	No			
		VCC_CLKIN3C					AD14	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCC_CLKIN4C					AC13	No			
		VCC_CLKIN7C					F14	No			
		VCC_CLKIN8C					F16	No			
		VCCBAT					H6	No			
		VCCA_PLL_B1					AC14	No			
		VCCA_PLL_L2					R23	No			
		VCCA_PLL_T1					E15	No			
		VCCD_PLL_B1					AC15	No			
		VCCD_PLL_L2					P23	No			
		VCCD_PLL_T1					F15	No			
		VCCIO1A					J23	No			
		VCCIO1A					H26	No			
		VCCIO1A					E26	No			
		VCCIO1C					P24	No			
		VCCIO1C					N26	No			
		VCCIO2A					AD25	No			
		VCCIO2A					AB26	No			
		VCCIO2A					AA23	No			
		VCCIO2C					T24	No			
		VCCIO2C					T26	No			
		VCCIO3A					AF20	No			
		VCCIO3A					AF23	No			
		VCCIO3A					AC20	No			
		VCCIO3A					Y19	No			
		VCCIO3C					AF17	No			
		VCCIO3C					AC17	No			
		VCCIO4A					AF5	No			
		VCCIO4A					AF8	No			
		VCCIO4A					AC7	No			
		VCCIO4A					AC9	No			
		VCCIO4C					AF13	No			
		VCCIO4C					AC11	No			
		VCCIO7A					J10	No			
		VCCIO7A					F9	No			
		VCCIO7A					C6	No			
		VCCIO7A					C9	No			
		VCCIO7C					F12	No			
		VCCIO7C					C12	No			
		VCCIO8A					J19	No			
		VCCIO8A					F22	No			
		VCCIO8A					E24	No			
		VCCIO8A					C23	No			
		VCCIO8C					G18	No			
		VCCIO8C					C16	No			
		VCCPD1A					L19	No			
		VCCPD1C					N19	No			
		VCCPD2A					U19	No			
		VCCPD2C					R19	No			
		VCCPD3A					W17	No			
		VCCPD3C					W15	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCPD4A					W11	No			
		VCCPD4C					W13	No			
		VCCPD7A					K12	No			
		VCCPD7C					K14	No			
		VCCPD8A					K18	No			
		VCCPD8C					K16	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				J22	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				M22	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB19	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AB16	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB8	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AB13	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G10	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G13	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G20	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G16	No			
		NC					F23	No			
		NC					AE26	No			
		NC					AB6	No			
		NC					J8	No			
		NC					AE4	No			
		NC					AE3	No			
		NC					AE5	No			
		NC					AD5	No			
		NC					AC5	No			
		NC					AB5	No			
		NC					AA5	No			
		NC					Y5	No			
		NC					W5	No			
		NC					W10	No			
		NC					V7	No			
		NC					V8	No			
		NC					V10	No			
		NC					U9	No			
		NC					U10	No			
		NC					U20	No			
		NC					T9	No			
		NC					T10	No			
		NC					N10	No			
		NC					M9	No			
		NC					M10	No			
		NC					M20	No			
		NC					L7	No			
		NC					L9	No			
		NC					L10	No			
		NC					K5	No			
		NC					K6	No			
		NC					K7	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		NC					K8	No			
		NC					K10	No			
		NC					K20	No			
		NC					J5	No			
		NC					J6	No			
		NC					G5	No			
		NC					F5	No			
		NC					C3	No			
		NC					B1	No			
		VCCAUX					G22	No			
		VCCAUX					AB22	No			
		VCCAUX					AA7	No			
		VCCAUX					G7	No			
		VCCA_R					N6	No			
		VCCA_R					T5	No			
		VCCH_GXBR0					V5	No			
		VCCH_GXBR1					L6	No			
		VCCL_GXBR0					R8	No			
		VCCL_GXBR0					T7	No			
		VCCL_GXBR1					N8	No			
		VCCL_GXBR1					P7	No			
		VCCR_R					M5	No			
		VCCR_R					R6	No			
		VCCT_R					P5	No			
		VCCT_R					U6	No			
		VCCHIP_R					N9	No			
		VCCHIP_R					P9	No			
		VCCHIP_R					R9	No			
		RREF_R0					AF1	No			
		RREF_R1					D1	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1A		TDI		TDI			B32	No			
1A		TMS		TMS			A33	No			
1A		TRST		TRST			C32	No			
1A		TCK		TCK			B34	No			
1A		TDO		TDO			B33	No			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	K24	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	L24	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	D29	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	C28	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	L23	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	M23	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	E29	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D28	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	J26	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	K25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C30	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	C29	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	K27	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	K26	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F29	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F28	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	P24	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	P23	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G29	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G28	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	J25	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	H24	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	H27	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	G26	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	J27	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	H26	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	G27	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F26	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	M24	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	N23	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	J30	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	H29	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N26	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	N25	Yes			
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	J29	Yes	DQSn5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	J28	Yes	DQS5L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	N27	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	M26	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	L27	Yes	DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	L26	Yes	DQ5L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	P26	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	R25	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	K30	Yes	DQSn6L	DQ5L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	L30	Yes	DQS6L	DQ5L/CQn5L	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	U25	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	T24	Yes	DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	K29	Yes	DQSn7L	DQSn5L/DQ5L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	K28	Yes	DQS7L	DQS5L/CQ5L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	R24	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	R23	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	M30	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	L29	Yes	DQ7L	DQ5L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	M29	No			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	M28	No			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	T26	No			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	U26	No			
1C	VREFB1CN0	CLK1n	CLK1n				N29	No			
1C	VREFB1CN0	CLK1p	CLK1p				N28	No			
2C	VREFB2CN0	CLK3p	CLK3p				AA28	No			
2C	VREFB2CN0	CLK3n	CLK3n				AA29	No			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	AC29	No			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	AB29	No			
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	W24	No			
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	V25	No			
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	AB27	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	AC28	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	AA26	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	AA27	Yes	DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	AD26	Yes	DQS8L	DQS10L/CQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	AE27	Yes	DQSn8L	DQSn10L/DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	Y22	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	W23	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	AC26	Yes	DQS9L	DQ10L/CQn10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	AD27	Yes	DQSn9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	Y23	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	Y24	Yes	DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	AF28	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	AE29	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	AC25	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	AB26	Yes	DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	AE28	Yes	DQS10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	AD29	Yes	DQSn10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	AA24	Yes			
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	Y25	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L21p	DIFFOUT_L41p	AG29	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L21n	DIFFOUT_L41n	AF29	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L21p	DIFFOUT_L42p	AE23	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L21n	DIFFOUT_L42n	AD24	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L22p	DIFFOUT_L43p	AJ26	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L22n	DIFFOUT_L43n	AK27	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22p	DIFFOUT_L44p	AG24	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22n	DIFFOUT_L44n	AF25	Yes	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	AH26	Yes	DQS11L	DQS13L/CQ13L	DQ14L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	AJ27	Yes	DQSn11L	DQSn13L/DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	AG23	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	AF24	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AH28	Yes	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AH29	Yes	DQSn12L	DQ13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AF26	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AF27	Yes	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AJ28	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AJ29	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AG26	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AG27	Yes	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AM29	Yes	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AM30	Yes	DQSn13L	DQSn14L/DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	AF23	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	AE24	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AM28	Yes	DQS14L	DQ14L/CQn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AL29	Yes	DQSn14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AB23	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AA23	Yes	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AL28	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AK29	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AD23	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AC24	Yes			
		nCONFIG		nCONFIG			AM34	No			
		nSTATUS		nSTATUS			AM33	No			
		CONF_DONE		CONF_DONE			AL32	No			
		PORSEL					AN33	No			
		nCE		nCE			AN34	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AP31	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AP29	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AP30	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AN30	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AN29	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AP28	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AP27	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AN27	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AM26	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AP25	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AP26	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AN26	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AL26	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AL27	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AM25	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AL25	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AJ25	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AH25	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AK23	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AJ23	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AH24	Yes	DQ4B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH23	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AL24	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AK24	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AL22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AJ21	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AM23	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL23	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AH22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AJ22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP24	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AN24	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AM22	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AP22	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP23	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AN23	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AH20	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AF20	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AG21	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AF21	Yes			
3C	VREFB3CN0	IO				DIFFOUT_B21n	AN21	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B21p	AP21	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AL21	Yes	DQSn7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AK21	Yes	DQS7B	DQ7B/CQn7B	
3C	VREFB3CN0	IO				DIFFOUT_B23n	AM21	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B23p	AM20	Yes	DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AL20	Yes	DQSn8B	DQSn7B/DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AK20	Yes	DQS8B	DQS7B/CQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25n	AJ20	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25p	AJ19	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AM19	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AL19	Yes	DQ8B	DQ7B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AC18	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AD18	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AF19	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AE19	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AF18	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	AE18	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AM18	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AL18	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AP20	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AN20	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AP18	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AN18	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AN15	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AP15	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AN17	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AP17	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AE17	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AF17	Yes			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
4C	VREFB4CN0	IO				DIFFOUT_B36p	AH16	Yes	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B36n	AJ15	Yes	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AE16	Yes	DQS9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AF16	Yes	DQSn9B		
4C	VREFB4CN0	IO				DIFFOUT_B38p	AD17	Yes	DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B38n	AK17	Yes	DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AL16	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AM16	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40p	AM17	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40n	AL17	Yes	DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AK15	Yes	DQS10B	DQS11B/CQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AL15	Yes	DQSn10B	DQSn11B/DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42p	AM14	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42n	AM15	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AK14	Yes	DQS11B	DQ11B/CQn11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AL14	Yes	DQSn11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44p	AN14	Yes	DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44n	AP14	Yes	DQ11B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	AE15	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	AF15	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B46p	AF14	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B46n	AG15	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AN12	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AP12	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48p	AM13	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48n	AP13	Yes	DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AN11	Yes	DQS12B	DQS15B/CQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AP11	Yes	DQSn12B	DQSn15B/DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50p	AJ12	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50n	AL13	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AL11	Yes	DQS13B	DQ15B/CQn15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AM11	Yes	DQSn13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52p	AK12	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52n	AL12	Yes	DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AH13	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AJ13	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54p	AH11	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54n	AH12	Yes	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AH14	Yes	DQS14B	DQS16B/CQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AJ14	Yes	DQSn14B	DQSn16B/DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56p	AJ10	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56n	AK11	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AL10	Yes	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AM10	Yes	DQSn15B	DQ16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58p	AL9	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58n	AL8	Yes	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AN9	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AP9	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AM8	Yes	DQ16B	DQ17B	DQ17B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
4A	VREFB4AN0	IO				DIFFOUT_B60n	AP10	Yes	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AN8	Yes	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AP8	Yes	DQSn16B	DQSn17B/DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AN6	Yes	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AP7	Yes	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AN5	Yes	DQS17B	DQ17B/CQn17B	DQ17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AP5	Yes	DQSn17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	AP4	Yes	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AP6	Yes	DQ17B	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			AN2	No			
		nCEO		nCEO			AL3	No			
		DCLK		DCLK			AM3	No			
		nCSO		nCSO			AM2	No			
		ASDO		ASDO			AM1	No			
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AC11	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AC12	Yes			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AL6	Yes			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AM7	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB12	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AA12	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AM5	Yes	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AM6	Yes	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AF11	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AE12	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AL5	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AK6	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AE8	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AF9	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AH7	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AJ8	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AE9	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AE10	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AJ6	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AJ7	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AG12	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AF12	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AH8	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AJ9	Yes	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AF10	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AG11	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AL7	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AK8	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AD11	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AD12	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AG8	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AG9	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AB10	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AB11	Yes			
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AE6	Yes	DQSn5R		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AF7	Yes	DQS5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AB9	Yes	DQ5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AC10	Yes	DQ5R		
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AG6	Yes	DQ5R		
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AF6	Yes	DQ5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	Y10	Yes	DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AA11	Yes	DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AD6	Yes	DQSn6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AE7	Yes	DQS6R	DQ5R/CQn5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	Y12	Yes	DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	W12	Yes	DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AD8	Yes	DQSn7R	DQSn5R/DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AD9	Yes	DQS7R	DQS5R/CQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AA8	Yes	DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AA9	Yes	DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AC7	Yes	DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AB8	Yes	DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	V10	No			
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	W11	No			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	AC6	No			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	AB6	No			
5C	VREFB5CN0	CLK8n	CLK8n				AA6	No			
5C	VREFB5CN0	CLK8p	CLK8p				AA7	No			
6C	VREFB6CN0	CLK10p	CLK10p				N7	No			
6C	VREFB6CN0	CLK10n	CLK10n				N6	No			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	M6	No			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	M5	No			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	T9	No			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	U9	No			
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	M7	Yes	DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	L6	Yes	DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	R11	Yes	DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	R10	Yes	DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	J5	Yes	DQS8R	DQS10R/CQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	K5	Yes	DQSn8R	DQSn10R/DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	T11	Yes	DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	U10	Yes	DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	K6	Yes	DQS9R	DQ10R/CQn10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	L5	Yes	DQSn9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	R13	Yes	DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	R12	Yes	DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	L9	Yes	DQ10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	M8	Yes	DQ10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	N9	Yes	DQ10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	N8	Yes	DQ10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	L8	Yes	DQS10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	K7	Yes	DQSn10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	N10	Yes			
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	P9	Yes			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
6A	VREFB6AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R41p	J7	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R41n	H6	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R21p	DIFFOUT_R42p	L11	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R21n	DIFFOUT_R42n	M10	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R22p	DIFFOUT_R43p	F9	Yes	DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R22n	DIFFOUT_R43n	G8	Yes	DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R22p	DIFFOUT_R44p	H9	Yes	DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R22n	DIFFOUT_R44n	J8	Yes	DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	G9	Yes	DQS11R	DQS13R/CQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	H8	Yes	DQSn11R	DQSn13R/DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	H11	Yes	DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	J10	Yes	DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	G7	Yes	DQS12R	DQ13R/CQn13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	G6	Yes	DQSn12R	DQ13R	DQSn14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	P12	Yes	DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	P11	Yes	DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	F7	Yes	DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	F6	Yes	DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	J9	Yes	DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	K8	Yes	DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	C6	Yes	DQS13R	DQS14R/CQ14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	C5	Yes	DQSn13R	DQSn14R/DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	K11	Yes	DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	K10	Yes	DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	D7	Yes	DQS14R	DQ14R/CQn14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	E6	Yes	DQSn14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	M12	Yes	DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	M11	Yes	DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	C7	Yes			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	D6	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	N12	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	N11	Yes			
		MSEL2		MSEL2			B1	No			
		MSEL1		MSEL1			C3	No			
		MSEL0		MSEL0			B2	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	A6	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	A4	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A5	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B5	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A7	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B6	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	A8	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	B8	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	A10	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	C9	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	A9	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	B9	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	E8	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	D8	Yes	DQ3T	DQ2T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	C10	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	D10	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	F10	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	D9	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	G12	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	H12	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	F13	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	G13	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	F11	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	G11	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	C12	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	D12	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	D11	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	E11	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	D13	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	E12	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A11	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B11	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	A13	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C13	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A12	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B12	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	F14	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	H14	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	H15	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J15	Yes			
7C	VREFB7CN0	IO				DIFFOUT_T21n	A14	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T21p	B14	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	D14	Yes	DQSn7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	E14	Yes	DQS7T	DQ7T/CQn7T	
7C	VREFB7CN0	IO				DIFFOUT_T23n	C15	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T23p	C14	Yes	DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	D15	Yes	DQSn8T	DQSn7T/DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	E15	Yes	DQS8T	DQS7T/CQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25n	D17	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25p	C17	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C16	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D16	Yes	DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T27n	E17	Yes	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T27p	L17	Yes	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	J16	Yes	DQSn9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	K16	Yes	DQS9T		
7C	VREFB7CN0	IO				DIFFOUT_T29n	F15	Yes	DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T29p	G16	Yes	DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	J17	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	K17	Yes			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A17	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B17	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A15	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	B15	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	B18	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A18	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B20	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A20	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	D18	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	C18	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	K18	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	J18	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	K19	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	J19	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	L18	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	M18	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	D19	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	C19	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40p	F19	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40n	F20	Yes	DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	E20	Yes	DQS10T	DQS11T/CQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	D20	Yes	DQSn10T	DQSn11T/DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42p	C20	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42n	C21	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	E21	Yes	DQS11T	DQ11T/CQn11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	D21	Yes	DQSn11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44p	A21	Yes	DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44n	B21	Yes	DQ11T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	J21	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	H21	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T46p	J20	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T46n	G20	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	B23	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	A23	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48p	A22	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48n	C22	Yes	DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	B24	Yes	DQS12T	DQS15T/CQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	A24	Yes	DQSn12T	DQSn15T/DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50p	F22	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50n	G22	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	D23	Yes	DQS13T	DQ15T/CQn15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	C23	Yes	DQSn13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52p	F21	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52n	D22	Yes	DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	E24	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	D24	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54p	G23	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54n	G24	Yes	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	F23	Yes	DQS14T	DQS16T/CQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	E23	Yes	DQSn14T	DQSn16T/DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56p	G25	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56n	F25	Yes	DQ15T	DQ16T	DQ17T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	D25	Yes	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	C25	Yes	DQSn15T	DQ16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58p	D27	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58n	D26	Yes	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B26	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A26	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	A25	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	C26	Yes	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	B27	Yes	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	A27	Yes	DQSn16T	DQSn17T/DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	A28	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	B29	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	B30	Yes	DQS17T	DQ17T/CQn17T	DQ17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	A30	Yes	DQSn17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	A29	Yes	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	A31	Yes	DQ17T	DQ17T	DQ17T
QL1		GXB_TX_L7n					E32	No			
QL1		GXB_TX_L7p					E31	No			
QL1		GXB_RX_L7n					F34	No			
QL1		GXB_RX_L7p					F33	No			
QL1		GXB_TX_L6n					G32	No			
QL1		GXB_TX_L6p					G31	No			
QL1		GXB_RX_L6n					H34	No			
QL1		GXB_RX_L6p					H33	No			
QL1		GXB_CMUTX_L3n					J32	No			
QL1		GXB_CMUTX_L3p					J31	No			
QL1		REFCLK_L3n,GXB_CMURX_L3n					K34	No			
QL1		REFCLK_L3p,GXB_CMURX_L3p					K33	No			
QL1		GXB_CMUTX_L2n					L32	No			
QL1		GXB_CMUTX_L2p					L31	No			
QL1		REFCLK_L2n,GXB_CMURX_L2n					M34	No			
QL1		REFCLK_L2p,GXB_CMURX_L2p					M33	No			
QL1		GXB_TX_L5n					N32	No			
QL1		GXB_TX_L5p					N31	No			
QL1		GXB_RX_L5n					P34	No			
QL1		GXB_RX_L5p					P33	No			
QL1		GXB_TX_L4n					R32	No			
QL1		GXB_TX_L4p					R31	No			
QL1		GXB_RX_L4n					T34	No			
QL1		GXB_RX_L4p					T33	No			
QL0		GXB_TX_L3n					U32	No			
QL0		GXB_TX_L3p					U31	No			
QL0		GXB_RX_L3n					V34	No			
QL0		GXB_RX_L3p					V33	No			
QL0		GXB_TX_L2n					W32	No			
QL0		GXB_TX_L2p					W31	No			
QL0		GXB_RX_L2n					Y34	No			
QL0		GXB_RX_L2p					Y33	No			
QL0		GXB_CMUTX_L1n					AA32	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
QL0		GXB_CMUTX_L1p					AA31	No			
QL0		REFCLK_L1n,GXB_CMURX_L1n					AB34	No			
QL0		REFCLK_L1p,GXB_CMURX_L1p					AB33	No			
QL0		GXB_CMUTX_L0n					AC32	No			
QL0		GXB_CMUTX_L0p					AC31	No			
QL0		REFCLK_L0n,GXB_CMURX_L0n					AD34	No			
QL0		REFCLK_L0p,GXB_CMURX_L0p					AD33	No			
QL0		GXB_TX_L1n					AE32	No			
QL0		GXB_TX_L1p					AE31	No			
QL0		GXB_RX_L1n					AF34	No			
QL0		GXB_RX_L1p					AF33	No			
QL0		GXB_TX_L0n					AG32	No			
QL0		GXB_TX_L0p					AG31	No			
QL0		GXB_RX_L0n					AH34	No			
QL0		GXB_RX_L0p					AH33	No			
QR0		GXB_RX_R0p					AH2	No			
QR0		GXB_RX_R0n					AH1	No			
QR0		GXB_TX_R0p					AG4	No			
QR0		GXB_TX_R0n					AG3	No			
QR0		GXB_RX_R1p					AF2	No			
QR0		GXB_RX_R1n					AF1	No			
QR0		GXB_TX_R1p					AE4	No			
QR0		GXB_TX_R1n					AE3	No			
QR0		REFCLK_R0p,GXB_CMURX_R0p					AD2	No			
QR0		REFCLK_R0n,GXB_CMURX_R0n					AD1	No			
QR0		GXB_CMUTX_R0p					AC4	No			
QR0		GXB_CMUTX_R0n					AC3	No			
QR0		REFCLK_R1p,GXB_CMURX_R1p					AB2	No			
QR0		REFCLK_R1n,GXB_CMURX_R1n					AB1	No			
QR0		GXB_CMUTX_R1p					AA4	No			
QR0		GXB_CMUTX_R1n					AA3	No			
QR0		GXB_RX_R2p					Y2	No			
QR0		GXB_RX_R2n					Y1	No			
QR0		GXB_TX_R2p					W4	No			
QR0		GXB_TX_R2n					W3	No			
QR0		GXB_RX_R3p					V2	No			
QR0		GXB_RX_R3n					V1	No			
QR0		GXB_TX_R3p					U4	No			
QR0		GXB_TX_R3n					U3	No			
QR1		GXB_RX_R4p					T2	No			
QR1		GXB_RX_R4n					T1	No			
QR1		GXB_TX_R4p					R4	No			
QR1		GXB_TX_R4n					R3	No			
QR1		GXB_RX_R5p					P2	No			
QR1		GXB_RX_R5n					P1	No			
QR1		GXB_TX_R5p					N4	No			
QR1		GXB_TX_R5n					N3	No			
QR1		REFCLK_R2p,GXB_CMURX_R2p					M2	No			
QR1		REFCLK_R2n,GXB_CMURX_R2n					M1	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
QR1		GXB_CMUTX_R2p					L4	No			
QR1		GXB_CMUTX_R2n					L3	No			
QR1		REFCLK_R3p,GXB_CMURX_R3p					K2	No			
QR1		REFCLK_R3n,GXB_CMURX_R3n					K1	No			
QR1		GXB_CMUTX_R3p					J4	No			
QR1		GXB_CMUTX_R3n					J3	No			
QR1		GXB_RX_R6p					H2	No			
QR1		GXB_RX_R6n					H1	No			
QR1		GXB_TX_R6p					G4	No			
QR1		GXB_TX_R6n					G3	No			
QR1		GXB_RX_R7p					F2	No			
QR1		GXB_RX_R7n					F1	No			
QR1		GXB_TX_R7p					E4	No			
QR1		GXB_TX_R7n					E3	No			
		GND					AN1	No			
		GND					U18	No			
		GND					AN4	No			
		GND					AN7	No			
		GND					AN10	No			
		GND					AN13	No			
		GND					AN16	No			
		GND					AN19	No			
		GND					AN22	No			
		GND					AN25	No			
		GND					AN28	No			
		GND					AN31	No			
		GND					AK4	No			
		GND					AK7	No			
		GND					AK10	No			
		GND					AK13	No			
		GND					AK16	No			
		GND					AK19	No			
		GND					AK22	No			
		GND					AK25	No			
		GND					AK28	No			
		GND					AK31	No			
		GND					AG7	No			
		GND					AG10	No			
		GND					AG13	No			
		GND					AG16	No			
		GND					AG19	No			
		GND					AG22	No			
		GND					AG25	No			
		GND					AG28	No			
		GND					AD7	No			
		GND					AD10	No			
		GND					AD13	No			
		GND					AD16	No			
		GND					AD19	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					AD22	No			
		GND					AD25	No			
		GND					AD28	No			
		GND					AB7	No			
		GND					AB13	No			
		GND					AB15	No			
		GND					AB17	No			
		GND					AB19	No			
		GND					AB21	No			
		GND					AB28	No			
		GND					AA10	No			
		GND					AA14	No			
		GND					AA16	No			
		GND					AA18	No			
		GND					AA20	No			
		GND					AA22	No			
		GND					AA25	No			
		GND					Y13	No			
		GND					Y15	No			
		GND					Y17	No			
		GND					Y19	No			
		GND					Y21	No			
		GND					W10	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					W20	No			
		GND					W22	No			
		GND					W25	No			
		GND					V13	No			
		GND					V15	No			
		GND					V19	No			
		GND					V21	No			
		GND					U14	No			
		GND					U16	No			
		GND					U20	No			
		GND					U22	No			
		GND					T10	No			
		GND					T13	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					T21	No			
		GND					T25	No			
		GND					R14	No			
		GND					R16	No			
		GND					R18	No			
		GND					R20	No			
		GND					R22	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					P10	No			
		GND					P13	No			
		GND					P15	No			
		GND					P17	No			
		GND					P19	No			
		GND					P21	No			
		GND					P25	No			
		GND					N14	No			
		GND					N16	No			
		GND					N18	No			
		GND					N20	No			
		GND					N22	No			
		GND					L7	No			
		GND					L10	No			
		GND					L13	No			
		GND					L16	No			
		GND					L19	No			
		GND					L22	No			
		GND					L25	No			
		GND					L28	No			
		GND					H7	No			
		GND					H10	No			
		GND					H13	No			
		GND					H16	No			
		GND					H19	No			
		GND					H22	No			
		GND					H25	No			
		GND					H28	No			
		GND					E7	No			
		GND					E10	No			
		GND					E13	No			
		GND					E16	No			
		GND					E19	No			
		GND					E22	No			
		GND					E25	No			
		GND					E28	No			
		GND					B4	No			
		GND					B7	No			
		GND					B10	No			
		GND					B13	No			
		GND					B16	No			
		GND					B19	No			
		GND					B22	No			
		GND					B25	No			
		GND					B28	No			
		GND					B31	No			
		GND					C34	No			
		GND					C33	No			
		GND					D33	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					D32	No			
		GND					D31	No			
		GND					D30	No			
		GND					E34	No			
		GND					E33	No			
		GND					V27	No			
		GND					AL33	No			
		GND					AL34	No			
		GND					AK30	No			
		GND					AK33	No			
		GND					AJ30	No			
		GND					AJ33	No			
		GND					AJ34	No			
		GND					AH30	No			
		GND					AH31	No			
		GND					AH32	No			
		GND					AG30	No			
		GND					AG33	No			
		GND					AG34	No			
		GND					AF30	No			
		GND					AF31	No			
		GND					AF32	No			
		GND					AE30	No			
		GND					AE33	No			
		GND					AE34	No			
		GND					AD30	No			
		GND					AD31	No			
		GND					AD32	No			
		GND					AC33	No			
		GND					AC34	No			
		GND					AB30	No			
		GND					AB31	No			
		GND					AB32	No			
		GND					AA33	No			
		GND					AA34	No			
		GND					Y28	No			
		GND					Y29	No			
		GND					Y30	No			
		GND					Y31	No			
		GND					Y32	No			
		GND					W33	No			
		GND					W34	No			
		GND					V29	No			
		GND					V30	No			
		GND					V31	No			
		GND					V32	No			
		GND					U28	No			
		GND					U29	No			
		GND					U33	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					U34	No			
		GND					T30	No			
		GND					T31	No			
		GND					T32	No			
		GND					R27	No			
		GND					R29	No			
		GND					R33	No			
		GND					R34	No			
		GND					P27	No			
		GND					P28	No			
		GND					P29	No			
		GND					P30	No			
		GND					P31	No			
		GND					P32	No			
		GND					N33	No			
		GND					N34	No			
		GND					M31	No			
		GND					M32	No			
		GND					L33	No			
		GND					L34	No			
		GND					K31	No			
		GND					K32	No			
		GND					J33	No			
		GND					J34	No			
		GND					H30	No			
		GND					H31	No			
		GND					H32	No			
		GND					G30	No			
		GND					G33	No			
		GND					G34	No			
		GND					F30	No			
		GND					F31	No			
		GND					F32	No			
		GND					E30	No			
		GND					AL1	No			
		GND					C2	No			
		GND					D5	No			
		GND					D4	No			
		GND					D3	No			
		GND					D2	No			
		GND					E5	No			
		GND					E2	No			
		GND					C1	No			
		GND					AL2	No			
		GND					AK2	No			
		GND					AK5	No			
		GND					AJ1	No			
		GND					AJ2	No			
		GND					AJ5	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					AH3	No			
		GND					AH4	No			
		GND					AH5	No			
		GND					AG1	No			
		GND					AG2	No			
		GND					AG5	No			
		GND					AF3	No			
		GND					AF4	No			
		GND					AF5	No			
		GND					AE1	No			
		GND					AE2	No			
		GND					AE5	No			
		GND					AD3	No			
		GND					AD4	No			
		GND					AD5	No			
		GND					AC1	No			
		GND					AC2	No			
		GND					AB3	No			
		GND					AB4	No			
		GND					AB5	No			
		GND					AA1	No			
		GND					AA2	No			
		GND					Y3	No			
		GND					Y4	No			
		GND					Y5	No			
		GND					Y6	No			
		GND					Y7	No			
		GND					W1	No			
		GND					W2	No			
		GND					V3	No			
		GND					V4	No			
		GND					V5	No			
		GND					V6	No			
		GND					V8	No			
		GND					U1	No			
		GND					U2	No			
		GND					U6	No			
		GND					U7	No			
		GND					T3	No			
		GND					T4	No			
		GND					T5	No			
		GND					R1	No			
		GND					R2	No			
		GND					R6	No			
		GND					R8	No			
		GND					P3	No			
		GND					P4	No			
		GND					P5	No			
		GND					P6	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					P7	No			
		GND					P8	No			
		GND					N1	No			
		GND					N2	No			
		GND					M3	No			
		GND					M4	No			
		GND					L1	No			
		GND					L2	No			
		GND					K3	No			
		GND					K4	No			
		GND					J1	No			
		GND					J2	No			
		GND					H3	No			
		GND					H4	No			
		GND					H5	No			
		GND					G1	No			
		GND					G2	No			
		GND					G5	No			
		GND					F3	No			
		GND					F4	No			
		GND					F5	No			
		GND					E1	No			
		VCC					U17	No			
		VCC					AA17	No			
		VCC					AA21	No			
		VCC					Y14	No			
		VCC					Y16	No			
		VCC					Y18	No			
		VCC					W17	No			
		VCC					W19	No			
		VCC					W21	No			
		VCC					V14	No			
		VCC					V16	No			
		VCC					V18	No			
		VCC					V20	No			
		VCC					U15	No			
		VCC					U19	No			
		VCC					U21	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					T18	No			
		VCC					R17	No			
		VCC					R19	No			
		VCC					R21	No			
		VCC					P14	No			
		VCC					P18	No			
		VCC					AA15	No			
		VCC					AA19	No			
		VCC					Y20	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCC					W15	No			
		VCC					T20	No			
		VCC					R15	No			
		VCC					P16	No			
		VCC					P20	No			
		VCC					U27	No			
		VCC					Y27	No			
		VCC					W27	No			
		VCC					T27	No			
		VCC					W8	No			
		VCC					Y8	No			
		VCC					U8	No			
		VCC					T8	No			
		VCCPT					U23	No			
		VCCPT					V23	No			
		VCCPT					AH17	No			
		VCCPT					V12	No			
		VCCPT					U12	No			
		VCCPT					G17	No			
		DNU					V17	No			
		VCCPGM					AK26	No			
		VCCPGM					AH10	No			
		TEMPDIODEn					A3	No			
		TEMPDIODEp					B3	No			
		VCC_CLKIN3C					AJ18	No			
		VCC_CLKIN4C					AG17	No			
		VCC_CLKIN7C					H17	No			
		VCC_CLKIN8C					F18	No			
		VCCBAT					E9	No			
		VCCA_PLL_B1					AH18	No			
		VCCA_PLL_L2					U24	No			
		VCCA_PLL_R2					V11	No			
		VCCA_PLL_T1					G18	No			
		VCCD_PLL_B1					AG18	No			
		VCCD_PLL_L2					V24	No			
		VCCD_PLL_R2					U11	No			
		VCCD_PLL_T1					H18	No			
		VCCIO1A					N24	No			
		VCCIO1A					J24	No			
		VCCIO1A					F27	No			
		VCCIO1C					T23	No			
		VCCIO1C					M27	No			
		VCCIO2A					AH27	No			
		VCCIO2A					AE26	No			
		VCCIO2A					AC23	No			
		VCCIO2C					AC27	No			
		VCCIO2C					AB24	No			
		VCCIO3A					AH21	No			
		VCCIO3A					AM24	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCIO3A					AM27	No			
		VCCIO3A					AJ24	No			
		VCCIO3C					AK18	No			
		VCCIO3C					AP19	No			
		VCCIO4A					AH15	No			
		VCCIO4A					AM9	No			
		VCCIO4A					AM12	No			
		VCCIO4A					AJ11	No			
		VCCIO4C					AJ17	No			
		VCCIO4C					AP16	No			
		VCCIO5A					AH6	No			
		VCCIO5A					AH9	No			
		VCCIO5A					AE11	No			
		VCCIO5C					AC8	No			
		VCCIO5C					Y11	No			
		VCCIO6A					J6	No			
		VCCIO6A					J11	No			
		VCCIO6A					F8	No			
		VCCIO6C					T12	No			
		VCCIO6C					M9	No			
		VCCIO7A					C11	No			
		VCCIO7A					G15	No			
		VCCIO7A					F12	No			
		VCCIO7A					C8	No			
		VCCIO7C					A16	No			
		VCCIO7C					F17	No			
		VCCIO8A					C27	No			
		VCCIO8A					G21	No			
		VCCIO8A					F24	No			
		VCCIO8A					C24	No			
		VCCIO8C					A19	No			
		VCCIO8C					E18	No			
		VCCPD1A					P22	No			
		VCCPD1C					T22	No			
		VCCPD2A					AB22	No			
		VCCPD2C					V22	No			
		VCCPD3A					AB20	No			
		VCCPD3C					AB18	No			
		VCCPD4A					AB14	No			
		VCCPD4C					AB16	No			
		VCCPD5A					AA13	No			
		VCCPD5C					W13	No			
		VCCPD6A					N13	No			
		VCCPD6C					U13	No			
		VCCPD7A					N15	No			
		VCCPD7C					N17	No			
		VCCPD8A					N21	No			
		VCCPD8C					N19	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				M25	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				R26	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AE25	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AB25	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AG20	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AH19	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AG14	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AJ16	No			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AF8	No			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AC9	No			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				K9	No			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				R9	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G14	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				F16	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				H20	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G19	No			
		NC					A32	No			
		NC					AP33	No			
		NC					AP2	No			
		NC					A2	No			
		NC					AJ31	No			
		NC					AJ32	No			
		NC					AJ3	No			
		NC					AJ4	No			
		NC					AP3	No			
		NC					AP32	No			
		NC					AN3	No			
		NC					AN32	No			
		NC					AM4	No			
		NC					AM31	No			
		NC					AM32	No			
		NC					AL4	No			
		NC					AL30	No			
		NC					AL31	No			
		NC					AK3	No			
		NC					AK32	No			
		NC					AF13	No			
		NC					AE13	No			
		NC					AE14	No			
		NC					AE20	No			
		NC					AE21	No			
		NC					AE22	No			
		NC					AD14	No			
		NC					AD15	No			
		NC					AD20	No			
		NC					AD21	No			
		NC					AC13	No			
		NC					AC14	No			
		NC					AC15	No			
		NC					AC16	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		NC					AC17	No			
		NC					AC19	No			
		NC					AC20	No			
		NC					AC21	No			
		NC					AC22	No			
		NC					M13	No			
		NC					M14	No			
		NC					M15	No			
		NC					M16	No			
		NC					M17	No			
		NC					M19	No			
		NC					M20	No			
		NC					M21	No			
		NC					M22	No			
		NC					L12	No			
		NC					L14	No			
		NC					L15	No			
		NC					L20	No			
		NC					L21	No			
		NC					K12	No			
		NC					K13	No			
		NC					K14	No			
		NC					K15	No			
		NC					K20	No			
		NC					K21	No			
		NC					K22	No			
		NC					K23	No			
		NC					J12	No			
		NC					J13	No			
		NC					J14	No			
		NC					J23	No			
		NC					H23	No			
		NC					E26	No			
		NC					E27	No			
		NC					C4	No			
		NC					C31	No			
		VCCAUX					J22	No			
		VCCAUX					AF22	No			
		VCCAUX					AK9	No			
		VCCAUX					G10	No			
		VCCA_L					AC30	No			
		VCCA_L					U30	No			
		VCCA_R					AC5	No			
		VCCA_R					U5	No			
		VCCH_GXBL0					W29	No			
		VCCH_GXBL1					T29	No			
		VCCH_GXBR0					W6	No			
		VCCH_GXBR1					T6	No			
		VCCL_GXBL0					V28	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCL_GXBL0					W28	No			
		VCCL_GXBL1					T28	No			
		VCCL_GXBL1					R28	No			
		VCCL_GXBR0					W7	No			
		VCCL_GXBR0					V7	No			
		VCCL_GXBR1					T7	No			
		VCCL_GXBR1					R7	No			
		VCCR_L					N30	No			
		VCCR_L					W30	No			
		VCCR_R					W5	No			
		VCCR_R					N5	No			
		VCCT_L					R30	No			
		VCCT_L					AA30	No			
		VCCT_R					R5	No			
		VCCT_R					AA5	No			
		VCCHIP_L					V26	No			
		VCCHIP_L					Y26	No			
		VCCHIP_L					W26	No			
		VCCHIP_R					W9	No			
		VCCHIP_R					Y9	No			
		VCCHIP_R					V9	No			
		RREF_L0					AK34	No			
		RREF_L1					D34	No			
		RREF_R0					AK1	No			
		RREF_R1					D1	No			

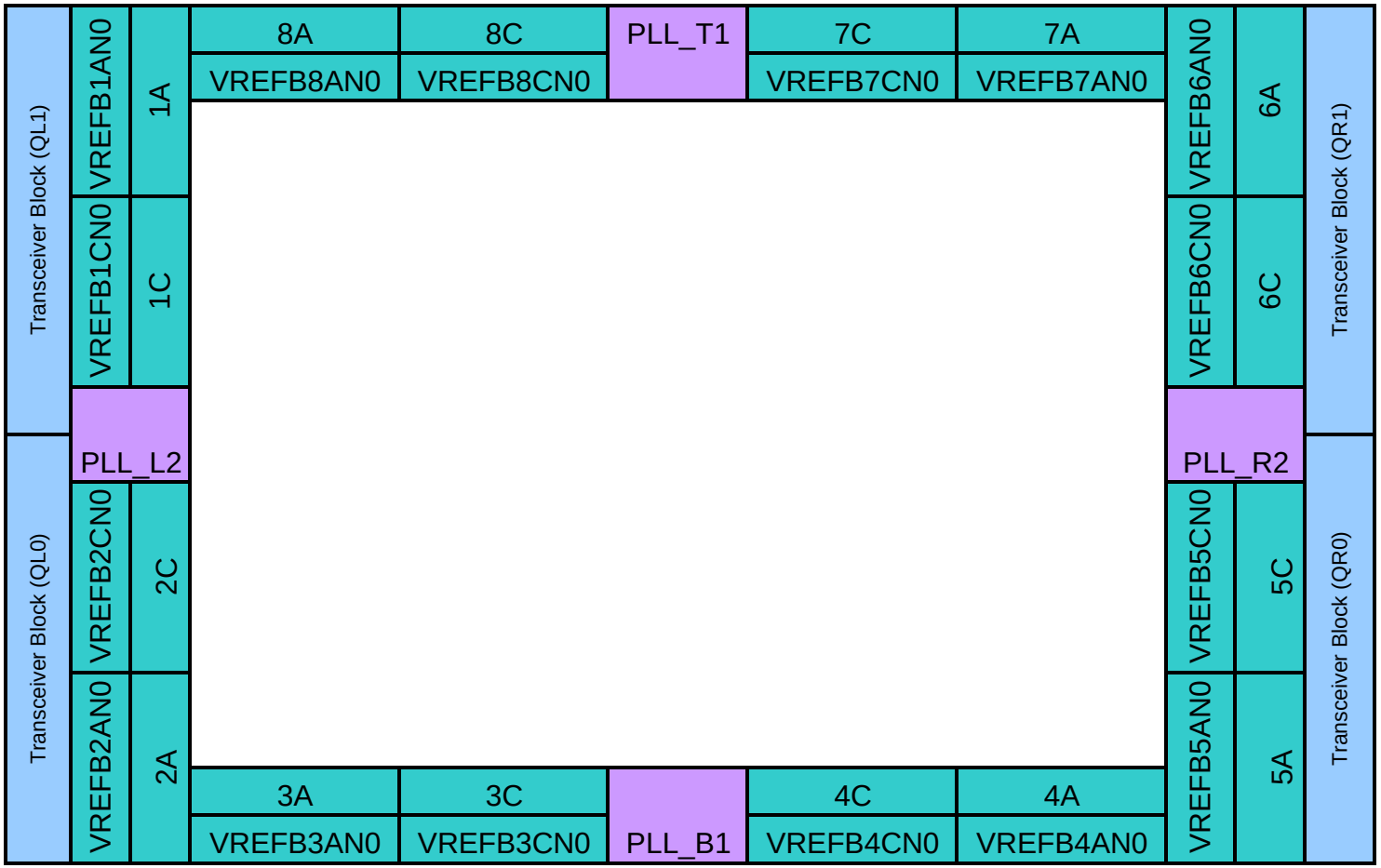
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Clock and PLL Pins
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
		Optional/Dual-Purpose Configuration Pins
CRC_ERROR (Note 6)	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DEV_CLRn (Note 6)	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE (Note 6)	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0 (Note 6)	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7] (Note 6)	I/O, Input	Dual-purpose configuration input data pins. The DATA[1:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE (Note 6)	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR (Note 6)	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p (Note 3)	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n (Note 3)	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p (Note 3)	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n (Note 3)	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p (Note 4 and 5)	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n (Note 4 and 5)	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p (Note 5) GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

1. This pin definition is prepared based on the EP4SGX530.
2. Some of the pull-up /pull-down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Stratix IV GX Devices chapter in the Stratix IV GX Device Handbook for more information.
3. Transceiver signals GXB_RX[0:15] and GXB_TX[0:15] are device specific.
4. Dual purpose CMU Receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th channels.
5. Only available in package with 5th and 6th channels.
6. These dual purpose configuration pins can only be used as configuration pins but not regular I/O in F780 of EP4SGX360 and EP4SGX290.
7. Refer to Pin Connections Guidelines and datasheet for the recommended operating voltage.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus ® II software for exact locations.

Version Number	Date	Changes Made
1.0	9/30/2008	Initial release.
1.1	12/30/2008	Updated VCCBAT from 2.5 V to 3.0 V.
1.2	6/9/2009	Added F1152 package and removed recommended operating voltage in pin definition.
1.3	12/3/2009	Added bank number for JTAG pins.
		Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.
1.4	2/4/2015	Added the Dynamic OCT Support columns in Pin List F780 and Pin List F1152.