Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					E33									
		DNU					F33									
		RREF_TL					F34									
GXB_L1		REFCLK3Ln					R27									
GXB_L1		REFCLK3Lp					R26									
GXB_L1		GXB_TX_L11n					G31									
GXB_L1		GXB_TX_L11p					G32									
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					H34									
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					H33									
GXB_L1		GXB_TX_L10n					J31									
GXB_L1		GXB_TX_L10p					J32									
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					K34									
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					K33									
GXB_L1		GXB_TX_L9n					L31									
GXB_L1		GXB_TX_L9p					L32									
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					M34									
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					M33									
GXB_L1		GXB_TX_L8n					N31									
GXB_L1		GXB_TX_L8p					N32									
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					P34									
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					P33									
GXB_L1		GXB_TX_L7n					R31									
GXB_L1		GXB_TX_L7p					R32									
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					T34									
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					T33									
GXB_L1		GXB_TX_L6n					U31									
GXB_L1		GXB_TX_L6p					U32									
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					V34									
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					V33									
GXB_L1		REFCLK2Ln					U27									
GXB_L1		REFCLK2Lp					U26									
GXB_L0		REFCLK1Ln					W27									
GXB_L0		REFCLK1Lp					W26									
GXB_L0		GXB_TX_L5n					W31									
GXB_L0		GXB_TX_L5p					W32									
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					Y34									
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					Y33									
GXB_L0		GXB_TX_L4n					AA31									
GXB_L0		GXB_TX_L4p					AA32									
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AB34									
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AB33									
GXB_L0		GXB_TX_L3n					AC31									
GXB_L0		GXB_TX_L3p					AC32									
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AD34									
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AD33									
GXB_L0		GXB_TX_L2n					AE31									
GXB_L0		GXB_TX_L2p					AE32									
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AF34									
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AF33									
GXB_L0		GXB_TX_L1n					AG31									
GXB_L0		GXB_TX_L1p					AG32									
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AH34									
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AH33									
GXB_L0		GXB_TX_L0n					AJ31									
GXB_L0		GXB_TX_L0p					AJ32									
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AK34									
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AK33									
GXB_L0		REFCLK0Ln					AA28									
GXB_L0		REFCLK0Lp					AA27									
		DNU					AL32									
3A		TDO		TDO			AM33									
3A		TMS		TMS			AD30									
3A		TCK		TCK			AM34									
3A		TDI		TDI			AN34									
3A		DCLK		DCLK			AP33									
3A		nCSO		DATA4			AC26									
3A		AS_DATA3		DATA3			AL31									
3A		AS_DATA2		DATA2			AM32									
3A		AS_DATA1		DATA1			AN33									
3A		AS_DATA0,ASDO		DATA0			AL30									
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AM30									
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AF29									
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AG29									
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AH29									
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AH28									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AJ29									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AK29									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AM31									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AN32									
3A	VREFB3AN0	IO	VREFB3AN0				AC27									
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AG27									
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AH27									
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AP32				CS# 3A_1	CS# 3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AP31	DQ1B	DQ1B		CS# 3A_0	CS# 3A_0				
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AG26	DQ1B	DQ1B							
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AH26	DQ1B	DQ1B							
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AE26				ODT_3A_1	ODT_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AF26	DQ1B	DQ1B		ODT 3A 0	ODT 3A 0				
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AL29	DQSn1B/QK1B	DQ1B		WE# 3A					
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AL28	DQS1B/CQ1B/CQn1B/QKn1B	DQ1B		CAS# 3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AN30				RAS# 3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AP30	DQ1B	DQ1B		BA 3A 2					
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AM28	DQ1B	DQ1B		BA 3A 1					
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AM29	DQ1B	DQ1B		BA 3A 0					
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AD27				A_3A_15					
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE27	DQ1B	DQ1B		A 3A 14					
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AJ27	DQ1B	DQ1B		A 3A 13					
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AK27	DQ1B	DQ1B		A 3A 12					
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AP29				A 3A 11					
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AP28	DQ2B	DQ1B		A 3A 10					
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AL27	DQ2B	DQ1B		A 3A 9	CA 3A 9				
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AM27	DQ2B	DQ1B		A 3A 8	CA 3A 8				
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AE28				A 3A 7	CA 3A 7				
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AF28	DQ2B	DQ1B		A 3A 6	CA 3A 6				
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AJ26	DQSn2B/QK2B	DQSn1B/QK1B		A 3A 5	CA 3A 5				
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AK26	DQS2B/CQ2B/CQn2B/QKn2B	DQS1B/CQ1B/CQn1B/QKn1B		A 3A 4	CA 3A 4				
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AN27				A 3A 3	CA 3A 3				
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AP27	DQ2B	DQ1B		A 3A 2	CA 3A 2				
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AL26	DQ2B	DQ1B		A 3A 1	CA 3A 1				
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AM26	DQ2B	DQ1B		A 3A 0	CA 3A 0				
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AD29				CKE_3A_1	CKE_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AE29	DQ2B	DQ1B		CKE_3A_0	CKE_3A_0				
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AN26	DQ2B	DQ1B		CK# 3A	CK# 3A				
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AP26	DQ2B	DQ1B		CK_3A	CK_3A				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AD26				RESET# 3A					
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE25	DQ3B	DQ2B	DQ1B	DQ1_3B_8	DQ1_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AE24	DQ3B	DQ2B	DQ1B	DQ1_3B_7	DQ1_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AF24	DQ3B	DQ2B	DQ1B	DQ1_3B_6	DQ1_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AB24									
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AB25	DQ3B	DQ2B	DQ1B	DM1_3B	DM1_3B				

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AC24	DQSn3B/QK3B	DQ2B	DQ1B	DQS#1_3B	DQS#1_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AD24	DQS3B/CQ3B/CQn3B/QKn3B	DQ2B	DQ1B	DQS1_3B	DQS1_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AH25									
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AJ25	DQ3B	DQ2B	DQ1B	DQ1_3B_5	DQ1_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AG24	DQ3B	DQ2B	DQ1B	DQ1_3B_4	DQ1_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AH24	DQ3B	DQ2B	DQ1B	DQ1_3B_3	DQ1_3B_3				
3B	VREFB3BN0	IO	VREFB3BN0				AC25									
3B	VREFB3BN0	IO					AC23	DQ3B	DQ2B	DQ1B	DQ1_3B_2	DQ1_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AL25	DQ3B	DQ2B	DQ1B	DQ1_3B_1	DQ1_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AL24	DQ3B	DQ2B	DQ1B	DQ1_3B_0	DQ1_3B_0				
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AJ24	DQ4B	DQ2B	DQ1B	DQ2_3B_8	DQ2_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AE23	DQ4B	DQ2B	DQ1B	DQ2_3B_7	DQ2_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AF23	DQ4B	DQ2B	DQ1B	DQ2_3B_6	DQ2_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ4B	DQ2B	DQ1B	DM2_3B	DM2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AP25	DQSn2B/QK4B	DQSn2B/QK2B	DQ1B	DQS#2_3B	DQS#2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AP24	DQS4B/CQ4B/CQn4B/QKn4B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2_3B	DQS2_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM25	DQ4B	DQ2B	DQ1B	DQ2_3B_5	DQ2_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AM23	DQ4B	DQ2B	DQ1B	DQ2_3B_4	DQ2_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AM24	DQ4B	DQ2B	DQ1B	DQ2_3B_3	DQ2_3B_3				
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ4B	DQ2B	DQ1B	DQ2_3B_2	DQ2_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AN23	DQ4B	DQ2B	DQ1B	DQ2_3B_1	DQ2_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ4B	DQ2B	DQ1B	DQ2_3B_0	DQ2_3B_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AF22	DQ5B	DQ3B	DQ1B	DQ3_3C_8	DQ3_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AG23	DQ5B	DQ3B	DQ1B	DQ3_3C_7	DQ3_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AH23	DQ5B	DQ3B	DQ1B	DQ3_3C_6	DQ3_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AE22	DQ5B	DQ3B	DQ1B	DM3_3C	DM3_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AJ23	DQSn5B/QK5B	DQ3B	DQSn1B/QK1B	DQS#3_3C	DQS#3_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AJ22	DQS5B/CQ5B/CQn5B/QKn5B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_3C	DQS3_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AH22	DQ5B	DQ3B	DQ1B	DQ3_3C_5	DQ3_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AG21	DQ5B	DQ3B	DQ1B	DQ3_3C_4	DQ3_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AH21	DQ5B	DQ3B	DQ1B	DQ3_3C_3	DQ3_3C_3				
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AC22	DQ5B	DQ3B	DQ1B	DQ3_3C_2	DQ3_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AK23	DQ5B	DQ3B	DQ1B	DQ3_3C_1	DQ3_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AL23	DQ5B	DQ3B	DQ1B	DQ3_3C_0	DQ3_3C_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AL22									
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AM22	DQ6B	DQ3B	DQ1B	DQ4_3C_8	DQ4_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN21	DQ6B	DQ3B	DQ1B	DQ4_3C_7	DQ4_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AP22	DQ6B	DQ3B	DQ1B	DQ4_3C_6	DQ4_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB21	DQ6B	DQ3B	DQ1B	DM4_3C	DM4_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AE21	DQSn6B/QK6B	DQSn3B/QK3B	DQ1B	DQS#4_3C	DQS#4_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE20	DQS6B/CQ6B/CQn6B/QKn6B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C	DQS4_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AL20	DQ6B	DQ3B	DQ1B	DQ4_3C_5	DQ4_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AF20	DQ6B	DQ3B	DQ1B	DQ4_3C_4	DQ4_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AG20	DQ6B	DQ3B	DQ1B	DQ4_3C_3	DQ4_3C_3				
3C	VREFB3CN0	IO	VREFB3CN0				AB22									
3C	VREFB3CN0	IO					AB20	DQ6B	DQ3B	DQ1B	DQ4_3C_2	DQ4_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AK21	DQ6B	DQ3B	DQ1B	DQ4_3C_1	DQ4_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AL21	DQ6B	DQ3B	DQ1B	DQ4_3C_0	DQ4_3C_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AH20	DQ7B			DQ5_3C_8	DQ5_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AJ20	DQ7B			DQ5_3C_7	DQ5_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AK20	DQ7B			DQ5_3C_6	DQ5_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC21	DQ7B			DM5_3C	DM5_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AP21	DQSn7B/QK7B			DQS#5_3C	DQS#5_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AP20	DQS7B/CQ7B/CQn7B/QKn7B			DQS5_3C	DQS5_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AM20	DQ7B			DQ5_3C_5	DQ5_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AN20	DQ7B			DQ5_3C_4	DQ5_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AP19	DQ7B			DQ5_3C_3	DQ5_3C_3				
3C	VREFB3CN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AC19	DQ7B			DQ5_3C_2	DQ5_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B61n	DIFFOUT_B61n	AC20	DQ7B			DQ5_3C_1	DQ5_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B61p	DIFFOUT_B61p	AD20	DQ7B			DQ5_3C_0	DQ5_3C_0				
3D	VREFB3DN0	IO	VREFB3DN0				AD18									
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AH19									
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AJ19									
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AL19									
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AM19									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AE19									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AF19									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AM18									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AN18									
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AJ18									
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AK18									
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AF18									
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AG18									
		VCCD_FPLL					AA17									
		VCCA_FPLL					AA18									
		DNU					AB19									
4D	VREFB4DN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AD17				CS#_4D_1	CS#_4D_1				
4D	VREFB4DN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AE17	DQ8B	DQ4B		CS#_4D_0	CS#_4D_0				
4D	VREFB4DN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AE16	DQ8B	DQ4B							
4D	VREFB4DN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AF16	DQ8B	DQ4B		A_4D_15					
4D	VREFB4DN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AB18				ODT_4D_1	ODT_4D_1				
4D	VREFB4DN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AC18	DQ8B	DQ4B		ODT_4D_0	ODT_4D_0				
4D	VREFB4DN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AF17	DQSn8B/QK8B	DQ4B		WE#_4D					
4D	VREFB4DN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AG17	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B		CAS#_4D					
4D	VREFB4DN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AH17				RAS#_4D					
4D	VREFB4DN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AH16	DQ8B	DQ4B		BA_4D_2					
4D	VREFB4DN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AJ16	DQ8B	DQ4B		BA_4D_1					
4D	VREFB4DN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AJ17	DQ8B	DQ4B		BA_4D_0					
4D	VREFB4DN0	IO	VREFB4DN0				AB17									
4D	VREFB4DN0	IO					AC17	DQ8B	DQ4B		A_4D_14					
4D	VREFB4DN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AK17	DQ8B	DQ4B		A_4D_13					
4D	VREFB4DN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AL16	DQ8B	DQ4B		A_4D_12					
4D	VREFB4DN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AL17				A_4D_11					
4D	VREFB4DN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AM17	DQ9B	DQ4B		A_4D_10					
4D	VREFB4DN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AP17	DQ9B	DQ4B		A_4D_9	CA_4D_9				
4D	VREFB4DN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AP18	DQ9B	DQ4B		A_4D_8	CA_4D_8				
4D	VREFB4DN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AB16				A_4D_7	CA_4D_7				
4D	VREFB4DN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AC16	DQ9B	DQ4B		A_4D_6	CA_4D_6				
4D	VREFB4DN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AP16	DQSn9B/QK9B	DQSn4B/QK4B		A_4D_5	CA_4D_5				
4D	VREFB4DN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AP15	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B		A_4D_4	CA_4D_4				
4D	VREFB4DN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AG15				A_4D_3	CA_4D_3				
4D	VREFB4DN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AH15	DQ9B	DQ4B		A_4D_2	CA_4D_2				
4D	VREFB4DN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AK15	DQ9B	DQ4B		A_4D_1	CA_4D_1				
4D	VREFB4DN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AL15	DQ9B	DQ4B		A_4D_0	CA_4D_0				
4D	VREFB4DN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AD15				CKE_4D_1	CKE_4D_1				
4D	VREFB4DN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AE15	DQ9B	DQ4B		CKE_4D_0	CKE_4D_0				
4D	VREFB4DN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AM16	DQ9B	DQ4B		CK#_4D	CK#_4D				
4D	VREFB4DN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AN15	DQ9B	DQ4B		CK_4D	CK_4D				
4C	VREFB4CN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AN14				RESET#_4D					
4C	VREFB4CN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AP14	DQ10B	DQ5B	DQ2B	DQ1_4C_8	DQ1_4C_8				
4C	VREFB4CN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AL14	DQ10B	DQ5B	DQ2B	DQ1_4C_7	DQ1_4C_7				
4C	VREFB4CN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AM14	DQ10B	DQ5B	DQ2B	DQ1_4C_6	DQ1_4C_6				
4C	VREFB4CN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AC15	DQ10B	DQ5B	DQ2B	DM1_4C	DM1_4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AJ14	DQSn10B/QK10B	DQ5B	DQ2B	DQS#1_4C	DQS#1_4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AK14	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B	DQ2B	DQS1_4C	DQS1_4C				
4C	VREFB4CN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AH14	DQ10B	DQ5B	DQ2B	DQ1_4C_5	DQ1_4C_5				
4C	VREFB4CN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AH13	DQ10B	DQ5B	DQ2B	DQ1_4C_4	DQ1_4C_4				
4C	VREFB4CN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AJ13	DQ10B	DQ5B	DQ2B	DQ1_4C_3	DQ1_4C_3				
4C	VREFB4CN0	IO	VREFB4CN0				AB15									
4C	VREFB4CN0	IO					AC13	DQ10B	DQ5B	DQ2B	DQ1_4C_2	DQ1_4C_2				

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4C	VREFB4CN0	IO			DIFFIO_RX_B114n	DIFFOUT_B114n	AC14	DQ10B	DQ5B	DQ2B	DQ1_4C_1	DQ1_4C_1				
4C	VREFB4CN0	IO			DIFFIO_RX_B114p	DIFFOUT_B114p	AD14	DQ10B	DQ5B	DQ2B	DQ1_4C_0	DQ1_4C_0				
4C	VREFB4CN0	IO			DIFFIO_TX_B115p	DIFFOUT_B115p	AF14	DQ11B	DQ5B	DQ2B	DQ2_4C_8	DQ2_4C_8				
4C	VREFB4CN0	IO			DIFFIO_RX_B116n	DIFFOUT_B116n	AL13	DQ11B	DQ5B	DQ2B	DQ2_4C_7	DQ2_4C_7				
4C	VREFB4CN0	IO			DIFFIO_RX_B116p	DIFFOUT_B116p	AM13	DQ11B	DQ5B	DQ2B	DQ2_4C_6	DQ2_4C_6				
4C	VREFB4CN0	IO			DIFFIO_TX_B117p	DIFFOUT_B117p	AB14	DQ11B	DQ5B	DQ2B	DM2_4C	DM2_4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B118n	DIFFOUT_B118n	AJ12	DQSn11B/QK11B		DQ2B	DQS#2_4C	DQS#2_4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B118p	DIFFOUT_B118p	AK12	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B	DQS2_4C	DQS2_4C				
4C	VREFB4CN0	IO			DIFFIO_TX_B119p	DIFFOUT_B119p	AG14	DQ11B	DQ5B	DQ2B	DQ2_4C_5	DQ2_4C_5				
4C	VREFB4CN0	IO			DIFFIO_RX_B120n	DIFFOUT_B120n	AE14	DQ11B	DQ5B	DQ2B	DQ2_4C_4	DQ2_4C_4				
4C	VREFB4CN0	IO			DIFFIO_RX_B120p	DIFFOUT_B120p	AF13	DQ11B	DQ5B	DQ2B	DQ2_4C_3	DQ2_4C_3				
4C	VREFB4CN0	IO			DIFFIO_TX_B121p	DIFFOUT_B121p	AB13	DQ11B	DQ5B	DQ2B	DQ2_4C_2	DQ2_4C_2				
4C	VREFB4CN0	IO			DIFFIO_RX_B122n	DIFFOUT_B122n	AF12	DQ11B	DQ5B	DQ2B	DQ2_4C_1	DQ2_4C_1				
4C	VREFB4CN0	IO			DIFFIO_RX_B122p	DIFFOUT_B122p	AG12	DQ11B	DQ5B	DQ2B	DQ2_4C_0	DQ2_4C_0				
4B	VREFB4BN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AP13	DQ12B	DQ6B	DQ2B	DQ3_4B_8	DQ3_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B124n	DIFFOUT_B124n	AN12	DQ12B	DQ6B	DQ2B	DQ3_4B_7	DQ3_4B_7				
4B	VREFB4BN0	IO			DIFFIO_RX_B124p	DIFFOUT_B124p	AP12	DQ12B	DQ6B	DQ2B	DQ3_4B_6	DQ3_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AE12	DQ12B	DQ6B	DQ2B	DM3_4B	DM3_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B126n	DIFFOUT_B126n	AM12	DQSn12B/QK12B	DQ6B		DQS#3_4B	DQS#3_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B126p	DIFFOUT_B126p	AN11	DQS12B/CQ12B/CQn12B/QKn12B	DQ6B		DQS3_4B	DQS3_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B127p	DIFFOUT_B127p	AL11	DQ12B	DQ6B	DQ2B	DQ3_4B_5	DQ3_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B128n	DIFFOUT_B128n	AG11	DQ12B	DQ6B	DQ2B	DQ3_4B_4	DQ3_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B128p	DIFFOUT_B128p	AH11	DQ12B	DQ6B	DQ2B	DQ3_4B_3	DQ3_4B_3				
4B	VREFB4BN0	IO			DIFFIO_TX_B129p	DIFFOUT_B129p	AD12	DQ12B	DQ6B	DQ2B	DQ3_4B_2	DQ3_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B130n	DIFFOUT_B130n	AL10	DQ12B	DQ6B	DQ2B	DQ3_4B_1	DQ3_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B130p	DIFFOUT_B130p	AM11	DQ12B	DQ6B	DQ2B	DQ3_4B_0	DQ3_4B_0				
4B	VREFB4BN0	IO			DIFFIO_TX_B131n	DIFFOUT_B131n	AP11									
4B	VREFB4BN0	IO			DIFFIO_TX_B131p	DIFFOUT_B131p	AP10	DQ13B	DQ6B	DQ2B	DQ4_4B_8	DQ4_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B132n	DIFFOUT_B132n	AJ11	DQ13B	DQ6B	DQ2B	DQ4_4B_7	DQ4_4B_7				
4B	VREFB4BN0	IO			DIFFIO_RX_B132p	DIFFOUT_B132p	AK11	DQ13B	DQ6B	DQ2B	DQ4_4B_6	DQ4_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B133p	DIFFOUT_B133p	AB12	DQ13B	DQ6B	DQ2B	DM4_4B	DM4_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B134n	DIFFOUT_B134n	AL9	DQSn13B/QK13B	DQSn6B/QK6B	DQ2B	DQS#4_4B	DQS#4_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B134p	DIFFOUT_B134p	AM10	DQS13B/CQ13B/CQn13B/QKn13B	DQS6B/CQ6B/CQn6B/QKn6B	DQ2B	DQS4_4B	DQS4_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B135p	DIFFOUT_B135p	AF11	DQ13B	DQ6B	DQ2B	DQ4_4B_5	DQ4_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B136n	DIFFOUT_B136n	AF9	DQ13B	DQ6B	DQ2B	DQ4_4B_4	DQ4_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B136p	DIFFOUT_B136p	AG9	DQ13B	DQ6B	DQ2B	DQ4_4B_3	DQ4_4B_3				
4B	VREFB4BN0	IO	VREFB4BN0				AA12									
4B	VREFB4BN0	IO					AC12	DQ13B	DQ6B	DQ2B	DQ4_4B_2	DQ4_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AD9	DQ13B	DQ6B	DQ2B	DQ4_4B_1	DQ4_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AE10	DQ13B	DQ6B	DQ2B	DQ4_4B_0	DQ4_4B_0				
4B	VREFB4BN0	IO			DIFFIO_TX_B138p	DIFFOUT_B138p	AE11	DQ14B	DQ7B		DQ5_4B_8	DQ5_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B139n	DIFFOUT_B139n	AJ9	DQ14B	DQ7B		DQ5_4B_7	DQ5_4B_7				
4B	VREFB4BN0	IO			DIFFIO_RX_B139p	DIFFOUT_B139p	AK9	DQ14B	DQ7B		DQ5_4B_6	DQ5_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B140p	DIFFOUT_B140p	AB11	DQ14B	DQ7B		DM5_4B	DM5_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B141n	DIFFOUT_B141n	AH10	DQSn14B/QK14B	DQ7B		DQS#5_4B	DQS#5_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B141p	DIFFOUT_B141p	AH9	DQS14B/CQ14B/CQn14B/QKn14B	DQ7B		DQS5_4B	DQS5_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B142p	DIFFOUT_B142p	AE9	DQ14B	DQ7B		DQ5_4B_5	DQ5_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B143n	DIFFOUT_B143n	AC9	DQ14B	DQ7B		DQ5_4B_4	DQ5_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B143p	DIFFOUT_B143p	AC8	DQ14B	DQ7B		DQ5_4B_3	DQ5_4B_3				
4B	VREFB4BN0	IO			DIFFIO_TX_B144p	DIFFOUT_B144p	AC11	DQ14B	DQ7B		DQ5_4B_2	DQ5_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B145n	DIFFOUT_B145n	AB10	DQ14B	DQ7B		DQ5_4B_1	DQ5_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B145p	DIFFOUT_B145p	AC10	DQ14B	DQ7B		DQ5_4B_0	DQ5_4B_0				
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B146p	DIFFOUT_B146p	AP9	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA11	DIFFIO_RX_B147n	DIFFOUT_B147n	AN8	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B147p	DIFFOUT_B147p	AN9	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA6	DIFFIO_TX_B148p	DIFFOUT_B148p	AF8	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA12	DIFFIO_RX_B149n	DIFFOUT_B149n	AL8	DQSn15B/QK15B	DQSn7B/QK7B							
4A	VREFB4AN0	IO		DATA13	DIFFIO_RX_B149p	DIFFOUT_B149p	AM8	DQS15B/CQ15B/CQn15B/QKn15B	DQS7B/CQ7B/CQn7B/QKn7B							
4A	VREFB4AN0	IO		DATA7	DIFFIO_TX_B150n	DIFFOUT_B150n	AP8									
4A	VREFB4AN0	IO		DATA8	DIFFIO_TX_B150p	DIFFOUT_B150p	AP7	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA14	DIFFIO_RX_B151n	DIFFOUT_B151n	AN6	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA15	DIFFIO_RX_B151p	DIFFOUT_B151p	AP6	DQ15B	DQ7B							
4A	VREFB4AN0	IO		DATA9	DIFFIO_TX_B152n	DIFFOUT_B152n	AE7									
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_TX_B152p	DIFFOUT_B152p	AF7	DQ15B	DQ7B							
4A	VREFB4AN0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AL7	DQ15B	DQ7B							
4A	VREFB4AN0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	AM7	DQ15B	DQ7B							
4A	VREFB4AN0	IO		PR_ERROR	DIFFIO_TX_B154n	DIFFOUT_B154n	AJ8									
4A	VREFB4AN0	IO		PR_READY	DIFFIO_TX_B154p	DIFFOUT_B154p	AK8	DQ16B								
4A	VREFB4AN0	IO		PR_DONE	DIFFIO_RX_B155n	DIFFOUT_B155n	AN5	DQ16B								
4A	VREFB4AN0	IO		PR_REQUEST	DIFFIO_RX_B155p	DIFFOUT_B155p	AP5	DQ16B								
4A	VREFB4AN0	IO		nPERSTR0	DIFFIO_TX_B156n	DIFFOUT_B156n	AD6									
4A	VREFB4AN0	IO		nPERSTL0	DIFFIO_TX_B156p	DIFFOUT_B156p	AE6	DQ16B								
4A	VREFB4AN0	IO		CvP_CONFDONE	DIFFIO_RX_B157n	DIFFOUT_B157n	AP4	DQSn16B/QK16B								
4A	VREFB4AN0	IO		CRC_ERROR	DIFFIO_RX_B157p	DIFFOUT_B157p	AP3	DQS16B/CQ16B/CQn16B/QKn16B								
4A	VREFB4AN0	IO		DEV_OE	DIFFIO_TX_B158n	DIFFOUT_B158n	AM6									
4A	VREFB4AN0	IO		DEV_CLRn	DIFFIO_TX_B158p	DIFFOUT_B158p	AM5	DQ16B								
4A	VREFB4AN0	IO		INIT_DONE	DIFFIO_RX_B159n	DIFFOUT_B159n	AK6	DQ16B								
4A	VREFB4AN0	IO		nCEO	DIFFIO_RX_B159p	DIFFOUT_B159p	AL6	DQ16B								
4A	VREFB4AN0	IO	VREFB4AN0				AC7									
4A	VREFB4AN0	IO					AD8	DQ16B								
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AH7	DQ16B								
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AJ7	DQ16B								
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AG8									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AH8									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AN3									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT_B162p	AP2									
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AM4									
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AM3									
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B166n	DIFFOUT_B166n	AL4									
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AL5									
4A	VREFB4AN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AF6									
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AG6									
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AH6									
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AJ6									
		RREF_BR					AM1									
		DNU					AM2									
		DNU					AN2									
GXB_R0		REFCLK0Rp					AA8									
GXB_R0		REFCLK0Rn					AA7									
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AK2									
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AK1									
GXB_R0		GXB_TX_R0p					AJ3									
GXB_R0		GXB_TX_R0n					AJ4									
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AH2									
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AH1									
GXB_R0		GXB_TX_R1p					AG3									
GXB_R0		GXB_TX_R1n					AG4									
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AF2									
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AF1									
GXB_R0		GXB_TX_R2p					AE3									
GXB_R0		GXB_TX_R2n					AE4									
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AD2									
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AD1									
GXB_R0		GXB_TX_R3p					AC3									
GXB_R0		GXB_TX_R3n					AC4									
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AB2									
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AB1									
GXB_R0		GXB_TX_R4p					AA3									
GXB_R0		GXB_TX_R4n					AA4									
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					V2									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					Y1									
GXB_R0		GXB_TX_R5p					W3									
GXB_R0		GXB_TX_R5n					W4									
GXB_R0		REFCLK1Rp					W8									
GXB_R0		REFCLK1Rn					W7									
6B	VREFB6BN0_HPS	HPS_DDR					T7				HPS_DM_4	HPS_DM_4				
6B	VREFB6BN0_HPS	HPS_DDR					T8				HPS_DQ_39	HPS_DQ_39				
6B	VREFB6BN0_HPS	HPS_DDR					U2				HPS_DQ_37	HPS_DQ_37				
6B	VREFB6BN0_HPS	HPS_DDR					V1				HPS_DQ_38	HPS_DQ_38				
6B	VREFB6BN0_HPS	HPS_DDR					U3				HPS_DQ_36	HPS_DQ_36				
6B	VREFB6BN0_HPS	HPS_DDR					T3				HPS_DQS_4	HPS_DQS_4				
6B	VREFB6BN0_HPS	HPS_GPI13					T1									
6B	VREFB6BN0_HPS	HPS_DDR					T4				HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6BN0_HPS	HPS_DDR					U1				HPS_DQ_35	HPS_DQ_35				
6B	VREFB6BN0_HPS	HPS_DDR					R1				HPS_DQ_33	HPS_DQ_33				
6B	VREFB6BN0_HPS	HPS_DDR					T5				HPS_DQ_34	HPS_DQ_34				
6B	VREFB6BN0_HPS	HPS_DDR					R2				HPS_DQ_32	HPS_DQ_32				
6B	VREFB6BN0_HPS	HPS_GPI12					T6									
6B	VREFB6BN0_HPS	HPS_GPI11					P1									
6B	VREFB6BN0_HPS	HPS_DDR					P2				HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0_HPS	HPS_GPI10					N1									
6B	VREFB6BN0_HPS	HPS_DDR					R3				HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0_HPS	HPS_DDR					N4				HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0_HPS	HPS_DDR					P7				HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0_HPS	HPS_DDR					P4				HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					R7									
6B	VREFB6BN0_HPS	HPS_DDR					L1				HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0_HPS	HPS_GPI9					M3									
6B	VREFB6BN0_HPS	HPS_DDR					M2				HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0_HPS	HPS_DDR					N3				HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0_HPS	HPS_DDR					K1				HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0_HPS	HPS_DDR					R4				HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0_HPS	HPS_DDR					L2				HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0_HPS	HPS_GPI8					P5									
6B	VREFB6BN0_HPS	HPS_GPI7					H2									
6B	VREFB6BN0_HPS	HPS_DDR					H1				HPS_DM_2	HPS_DM_2				
6B	VREFB6BN0_HPS	HPS_GPI6					J2									
6B	VREFB6BN0_HPS	HPS_DDR					J1				HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0_HPS	HPS_DDR					J3				HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0_HPS	HPS_DDR					N5				HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0_HPS	HPS_DDR					K3				HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0_HPS	HPS_GPI5					P6									
6B	VREFB6BN0_HPS	HPS_DDR					K4				HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0_HPS	HPS_DDR					L3				HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					L5				HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0_HPS	HPS_DDR					M4				HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					L6				HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0_HPS	HPS_DDR					N6				HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0_HPS	HPS_DDR					M6				HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0_HPS	HPS_GPI4					N7									
6A	VREFB6AN0_HPS	HPS_GPI3					G3									
6A	VREFB6AN0_HPS	HPS_DDR					F1				HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0_HPS	HPS_GPI2					H3									
6A	VREFB6AN0_HPS	HPS_DDR					G1				HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					H4				HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					K5				HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					J4				HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					K6				HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					D1				HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					E1				HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					C1				HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					E2				HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					F3				HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					J6				HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					F4				HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_GPI1					J7									
6A	VREFB6AN0_HPS	HPS_GPI0					C2									
6A	VREFB6AN0_HPS	HPS_DDR					G4				HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0_HPS	HPS_DDR					G5				HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					A2				HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					K7				HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					B1				HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					L7				HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					C3				HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0_HPS	HPS_DDR					E3				HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					D4				HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					E4				HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					A4				HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					M8				HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					A3				HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					N9									
6A	VREFB6AN0_HPS	HPS_DDR					B4				HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					C4				HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					D5				HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					J8				HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					E5				HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					K8				HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					A6				HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					B5				HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					B7				HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					B6				HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					C7				HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					G7				HPS_BA_0					
6A	VREFB6AN0_HPS	HPS_DDR					D6				HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					G6				HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					H6				HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					F6				HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					G8				HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					F7				HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					G9				HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					C8				HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					E7				HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					D7				HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					F8				HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					A8				HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					J9				HPS_WE#					
6A	VREFB6AN0_HPS	HPS_DDR					A7				HPS_A_15					
6A	VREFB6AN0_HPS	HPS_RZQ_0					K9									
		DNU					U4									
		GND					G10									
		GND					H10									
7A		HPS_nRST					P11									
7A		HPS_nPOR					F9									
7A		HPS_TDO					P10									
		VCCRSTCLK_HPS					E9									
7A		HPS_TMS					A9									
7A		HPS_TCK					C9									
7A		HPS_TRST					B10									
7A		HPS_TDI					D9									
		GND					N10									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A		HPS_PORSEL					C10									
7A		HPS_CLK1					L9									
7A		HPS_CLK2					D10									
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_CLK					A10						TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D0					K10						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D1					A11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D2					J10						TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D3					A12						TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D4					B12						TRACE_D4	SPIS1_CLK		HPS_GPIO53
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D5					A12						TRACE_D5	SPIS1_MOSI		HPS_GPIO54
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D6					C13						TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D7					C11						TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_CLK					L10						SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MOSI					C12						SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MISO					L11						SPIM0_MISO		UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0,BOOTSEL0					E10						SPIM0_SS0		UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX					E11						UART0_RX		SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX,CLKSEL1					F10						UART0_TX		SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SDA					F11						I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SCL					H11						I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX*					M10							UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX*,CLKSEL0					J11							UART0_TX	SPIM1_SS0	HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_CLK					M11						SPIS1_CLK	SPIM1_CLK		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MOSI					D12						SPIS1_MOSI	SPIM1_MOSI		HPS_GPIO68
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MISO					E12						SPIS1_MISO	SPIM1_MISO		HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_SS0					D13						SPIS1_SS0	SPIM1_SS0		HPS_GPIO70
7A	VREFB7A7B7C7D7EN0_HPS	UART1_RX					F12						UART1_RX	SPIM1_SS1		HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	UART1_TX					J12						UART1_TX	SPIM0_CLK		HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SDA					L12						I2C1_SDA	SPIM0_MOSI		HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SCL					K12						I2C1_SCL	SPIM0_MISO		HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0					M12							SPIM0_SS0		HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_CLK					F13						SPIS0_CLK	SPIM0_SS1		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MOSI					G12						SPIS0_MOSI			HPS_GPIO68
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MISO					G13						SPIS0_MISO			HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_SS0					H12						SPIS0_SS0			HPS_GPIO70
7B	VREFB7A7B7C7D7EN0_HPS	NAND_ALE					A14						NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CE					M13						NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CLE					B14						NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RE					N13						NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RB					B15						NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ0					C14						NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ1					C15						NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ2					D14						NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ3					G14						NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ4					N12						NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ5					H14						NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ6					P12						NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ7					K13						NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WP					J14						NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WE,BOOTSEL2					L14						NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO0					K14						QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO1					M14						QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO2					P14						QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO3					N14						QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS0,BOOTSEL1					R15						QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_CLK					F14						QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS1					D15						QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CMD					E15						SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_PWREN					J15						SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D0					F15						SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D1					K15						SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D4					E16						SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D5					G15						SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D6					F16						SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D7					G16						SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C7D7EN0_HPS	HPS_GPIO44					H16							USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CCLK_OUT					M15						SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D2					J16						SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D3					L15						SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CLK					A16						RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD0					A17						RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD1					A15						RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD2					B17						RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD3					C16						RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD0					L16						RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDIO					C17						RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDC					M16						RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CTL					D17						RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CTL					E18						RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CLK					D16						RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD1					F18						RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD2					F17						RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD3					P16						RGMII0_RXD3	USB1_NXT		HPS_GPIO13
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CLK					G17						RGMII1_TX_CLK			HPS_GPIO48
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD0					N16						RGMII1_TXD0			HPS_GPIO49
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD1					J17						RGMII1_TXD1			HPS_GPIO50
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CTL					G18						RGMII1_TX_CTL			HPS_GPIO51
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD0					K17						RGMII1_RXD0			HPS_GPIO52
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD1					H17						RGMII1_RXD1			HPS_GPIO53
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDIO					L17						RGMII1_MDIO	SPIM0_CLK	SPIS0_CLK	HPS_GPIO54
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDC					N19						RGMII1_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS_GPIO55
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD2					M17						RGMII1_TXD2	SPIM0_MISO	SPIS0_MISO	HPS_GPIO56
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD3					N18						RGMII1_TXD3	SPIM0_SS0	SPIS0_SS0	HPS_GPIO57
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CLK					M18						RGMII1_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS_GPIO58
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CTL					J18						RGMII1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GPIO59
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD2					N17						RGMII1_RXD2	SPIS1_MISO	SPIM1_MISO	HPS_GPIO60
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD3					K18						RGMII1_RXD3	SPIS1_SS0	SPIM1_SS0	HPS_GPIO61
		VCCA_FPLL					T17									
		VCCD_FPLL					T16									
		DNU					P19									
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T31p	DIFFOUT_T31p	C18									
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T31n	DIFFOUT_T31n	D18									
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T33p	DIFFOUT_T33p	D19									
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T33n	DIFFOUT_T33n	E19									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T35p	DIFFOUT_T35p	A18									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T35n	DIFFOUT_T35n	B19									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T36p	DIFFOUT_T36p	G19									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T36n	DIFFOUT_T36n	H19									
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T37p	DIFFOUT_T37p	C20									
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T37n	DIFFOUT_T37n	D20									
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T39p	DIFFOUT_T39p	A20									
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T39n	DIFFOUT_T39n	A21									
8D	VREFB8DN0	IO					K19									
8D	VREFB8DN0	IO	VREFB8DN0				L19									
8C	VREFB8CN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	K20	DQ1T			DQ5_8C_0	DQ5_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	L20	DQ1T			DQ5_8C_1	DQ5_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	P20	DQ1T			DQ5_8C_2	DQ5_8C_2				
8C	VREFB8CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	E20	DQ1T			DQ5_8C_3	DQ5_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	F20	DQ1T			DQ5_8C_4	DQ5_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	G20	DQ1T			DQ5_8C_5	DQ5_8C_5				

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
8C	VREFB8CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	B21	DQS1T/CQ1T/CQn1T/QKn1T			DQS5_8C	DQS5_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	C21	DQSn1T/QK1T			DQS#5_8C	DQS#5_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	N20	DQ1T			DM5_8C	DM5_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	H21	DQ1T			DQ5_8C_6	DQ5_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	J20	DQ1T			DQ5_8C_7	DQ5_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	E21	DQ1T			DQ5_8C_8	DQ5_8C_8				
8C	VREFB8CN0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	J21	DQ2T	DQ1T	DQ1T	DQ4_8C_0	DQ4_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	K21	DQ2T	DQ1T	DQ1T	DQ4_8C_1	DQ4_8C_1				
8C	VREFB8CN0	IO					N21	DQ2T	DQ1T	DQ1T	DQ4_8C_2	DQ4_8C_2				
8C	VREFB8CN0	IO	VREFB8CN0				P21									
8C	VREFB8CN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	M21	DQ2T	DQ1T	DQ1T	DQ4_8C_3	DQ4_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	M20	DQ2T	DQ1T	DQ1T	DQ4_8C_4	DQ4_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	F21	DQ2T	DQ1T	DQ1T	DQ4_8C_5	DQ4_8C_5				
8C	VREFB8CN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	D22	DQS2T/CQ2T/CQn2T/QKn2T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T	DQS4_8C	DQS4_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	E22	DQSn2T/QK2T	DQSn1T/QK1T	DQ1T	DQS#4_8C	DQS#4_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	N22	DQ2T	DQ1T	DQ1T	DM4_8C	DM4_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	A24	DQ2T	DQ1T	DQ1T	DQ4_8C_6	DQ4_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	A23	DQ2T	DQ1T	DQ1T	DQ4_8C_7	DQ4_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	E23	DQ2T	DQ1T	DQ1T	DQ4_8C_8	DQ4_8C_8				
8C	VREFB8CN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	F23									
8C	VREFB8CN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	G23	DQ3T	DQ1T	DQ1T	DQ3_8C_0	DQ3_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	H23	DQ3T	DQ1T	DQ1T	DQ3_8C_1	DQ3_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	P22	DQ3T	DQ1T	DQ1T	DQ3_8C_2	DQ3_8C_2				
8C	VREFB8CN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	G22	DQ3T	DQ1T	DQ1T	DQ3_8C_3	DQ3_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	H22	DQ3T	DQ1T	DQ1T	DQ3_8C_4	DQ3_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	J23	DQ3T	DQ1T	DQ1T	DQ3_8C_5	DQ3_8C_5				
8C	VREFB8CN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	K22	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS1T/CQ1T/CQn1T/QKn1T	DQS3_8C	DQS3_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	L22	DQSn3T/QK3T	DQ1T	DQSn1T/QK1T	DQS#3_8C	DQS#3_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	N23	DQ3T	DQ1T	DQ1T	DM3_8C	DM3_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	L23	DQ3T	DQ1T	DQ1T	DQ3_8C_6	DQ3_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	M23	DQ3T	DQ1T	DQ1T	DQ3_8C_7	DQ3_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	K23	DQ3T	DQ1T	DQ1T	DQ3_8C_8	DQ3_8C_8				
8B	VREFB8BN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	B23	DQ4T	DQ2T	DQ1T	DQ2_8B_0	DQ2_8B_0				
8B	VREFB8BN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	C24	DQ4T	DQ2T	DQ1T	DQ2_8B_1	DQ2_8B_1				
8B	VREFB8BN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	M24	DQ4T	DQ2T	DQ1T	DQ2_8B_2	DQ2_8B_2				
8B	VREFB8BN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	C23	DQ4T	DQ2T	DQ1T	DQ2_8B_3	DQ2_8B_3				
8B	VREFB8BN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	D23	DQ4T	DQ2T	DQ1T	DQ2_8B_4	DQ2_8B_4				
8B	VREFB8BN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	G24	DQ4T	DQ2T	DQ1T	DQ2_8B_5	DQ2_8B_5				
8B	VREFB8BN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	C25	DQS4T/CQ4T/CQn4T/QKn4T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS2_8B	DQS2_8B				
8B	VREFB8BN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	D24	DQSn4T/QK4T	DQSn2T/QK2T	DQ1T	DQS#2_8B	DQS#2_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	P24	DQ4T	DQ2T	DQ1T	DM2_8B	DM2_8B				
8B	VREFB8BN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	E24	DQ4T	DQ2T	DQ1T	DQ2_8B_6	DQ2_8B_6				
8B	VREFB8BN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	D25	DQ4T	DQ2T	DQ1T	DQ2_8B_7	DQ2_8B_7				
8B	VREFB8BN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	H24	DQ4T	DQ2T	DQ1T	DQ2_8B_8	DQ2_8B_8				
8B	VREFB8BN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	A25	DQ5T	DQ2T	DQ1T	DQ1_8B_0	DQ1_8B_0				
8B	VREFB8BN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	A26	DQ5T	DQ2T	DQ1T	DQ1_8B_1	DQ1_8B_1				
8B	VREFB8BN0	IO					M25	DQ5T	DQ2T	DQ1T	DQ1_8B_2	DQ1_8B_2				
8B	VREFB8BN0	IO	VREFB8BN0				N25									
8B	VREFB8BN0	IO			DIFFIO_RX_T86p	DIFFOUT_T86p	B26	DQ5T	DQ2T	DQ1T	DQ1_8B_3	DQ1_8B_3				
8B	VREFB8BN0	IO			DIFFIO_RX_T86n	DIFFOUT_T86n	C26	DQ5T	DQ2T	DQ1T	DQ1_8B_4	DQ1_8B_4				
8B	VREFB8BN0	IO			DIFFIO_TX_T87p	DIFFOUT_T87p	A27	DQ5T	DQ2T	DQ1T	DQ1_8B_5	DQ1_8B_5				
8B	VREFB8BN0	IO			DIFFIO_TX_T87n	DIFFOUT_T87n	A28									
8B	VREFB8BN0	IO			DIFFIO_RX_T88p	DIFFOUT_T88p	D26	DQS5T/CQ5T/CQn5T/QKn5T	DQ2T	DQ1T	DQS1_8B	DQS1_8B				
8B	VREFB8BN0	IO			DIFFIO_RX_T88n	DIFFOUT_T88n	E26	DQSn5T/QK5T	DQ2T	DQ1T	DQS#1_8B	DQS#1_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T89p	DIFFOUT_T89p	K24	DQ5T	DQ2T	DQ1T	DM1_8B	DM1_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T89n	DIFFOUT_T89n	L24									
8B	VREFB8BN0	IO			DIFFIO_RX_T90p	DIFFOUT_T90p	F26	DQ5T	DQ2T	DQ1T	DQ1_8B_6	DQ1_8B_6				
8B	VREFB8BN0	IO			DIFFIO_RX_T90n	DIFFOUT_T90n	F25	DQ5T	DQ2T	DQ1T	DQ1_8B_7	DQ1_8B_7				
8B	VREFB8BN0	IO			DIFFIO_TX_T91p	DIFFOUT_T91p	G26	DQ5T	DQ2T	DQ1T	DQ1_8B_8	DQ1_8B_8				
8B	VREFB8BN0	IO			DIFFIO_TX_T91n	DIFFOUT_T91n	G25				RESET#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T92p	DIFFOUT_T92p	B27	DQ6T	DQ3T		CK_8A	CK_8A				
8A	VREFB8AN0	IO			DIFFIO_RX_T92n	DIFFOUT_T92n	C28	DQ6T	DQ3T		CK#_8A	CK#_8A				
8A	VREFB8AN0	IO			DIFFIO_TX_T93p	DIFFOUT_T93p	J25	DQ6T	DQ3T		CKE_8A_0	CKE_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T93n	DIFFOUT_T93n	K25				CKE_8A_1	CKE_8A_1				
8A	VREFB8AN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	B29	DQ6T	DQ3T		A_8A_0	CA_8A_0				
8A	VREFB8AN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	C29	DQ6T	DQ3T		A_8A_1	CA_8A_1				
8A	VREFB8AN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	A29	DQ6T	DQ3T		A_8A_2	CA_8A_2				
8A	VREFB8AN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	A30				A_8A_3	CA_8A_3				
8A	VREFB8AN0	IO			DIFFIO_RX_T96p	DIFFOUT_T96p	A31	DQS6T/CQ6T/CQn6T/QKn6T	DQS3T/CQ3T/CQn3T/QKn3T		A_8A_4	CA_8A_4				
8A	VREFB8AN0	IO			DIFFIO_RX_T96n	DIFFOUT_T96n	B30	DQSn6T/QK6T	DQSn3T/QK3T		A_8A_5	CA_8A_5				
8A	VREFB8AN0	IO			DIFFIO_TX_T97p	DIFFOUT_T97p	J26	DQ6T	DQ3T		A_8A_6	CA_8A_6				
8A	VREFB8AN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	K26				A_8A_7	CA_8A_7				
8A	VREFB8AN0	IO			DIFFIO_RX_T98p	DIFFOUT_T98p	A33	DQ6T	DQ3T		A_8A_8	CA_8A_8				
8A	VREFB8AN0	IO			DIFFIO_RX_T98n	DIFFOUT_T98n	A32	DQ6T	DQ3T		A_8A_9	CA_8A_9				
8A	VREFB8AN0	IO			DIFFIO_TX_T99p	DIFFOUT_T99p	C33	DQ6T	DQ3T		A_8A_10					
8A	VREFB8AN0	IO			DIFFIO_TX_T99n	DIFFOUT_T99n	B32				A_8A_11					
8A	VREFB8AN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	D27	DQ7T	DQ3T		A_8A_12					
8A	VREFB8AN0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	D28	DQ7T	DQ3T		A_8A_13					
8A	VREFB8AN0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	L26	DQ7T	DQ3T		A_8A_14					
8A	VREFB8AN0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	M26				A_8A_15					
8A	VREFB8AN0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	E27	DQ7T	DQ3T		BA_8A_0					
8A	VREFB8AN0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	F27	DQ7T	DQ3T		BA_8A_1					
8A	VREFB8AN0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	F28	DQ7T	DQ3T		BA_8A_2					
8A	VREFB8AN0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	G28				RAS#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	C32	DQS7T/CQ7T/CQn7T/QKn7T	DQ3T		CAS#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	C31	DQSn7T/QK7T	DQ3T		WE#_8A					
8A	VREFB8AN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	L27	DQ7T	DQ3T		ODT_8A_0	ODT_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	M28				ODT_8A_1	ODT_8A_1				
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T106p	DIFFOUT_T106p	D31	DQ7T	DQ3T							
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T106n	DIFFOUT_T106n	E31	DQ7T	DQ3T							
8A	VREFB8AN0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	E30	DQ7T	DQ3T		CS#_8A_0	CS#_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	F29				CS#_8A_1	CS#_8A_1				
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T108p	DIFFOUT_T108p	G29									
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T108n	DIFFOUT_T108n	H29									
8A	VREFB8AN0	IO	VREFB8AN0				N26									
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T109p	DIFFOUT_T109p	J29									
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T109n	DIFFOUT_T109n	J28									
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T110p	DIFFOUT_T110p	K29									
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T110n	DIFFOUT_T110n	L29									
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T111p	DIFFOUT_T111p	J27									
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T111n	DIFFOUT_T111n	K28									
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T113p	DIFFOUT_T113p	H26									
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T113n	DIFFOUT_T113n	H27									
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T114n	DIFFOUT_T114n	D29									
8A		MSEL0		MSEL0			B34									
8A		MSEL1		MSEL1			C34									
8A		MSEL2		MSEL2			D34									
8A		MSEL3		MSEL3			K30									
8A		MSEL4		MSEL4			D32									
8A		CONF_DONE		CONF_DONE			D33									
8A		nSTATUS		nSTATUS			N27									
8A		nCE		nCE			H30									
8A		nCONFIG		nCONFIG			M29									
		GND					F30									
		VCC_HPS					U16									
		GND					U15									
		GND					AA26									
		GND					AA29									
		GND					AA33									
		GND					AA34									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AB27									
		GND					AB28									
		GND					AB30									
		GND					AB31									
		GND					AB32									
		GND					AC30									
		GND					AC33									
		GND					AC34									
		GND					AD31									
		GND					AD32									
		GND					AE30									
		GND					AE33									
		GND					AE34									
		GND					AF31									
		GND					AF32									
		GND					AG30									
		GND					AG33									
		GND					AG34									
		GND					AH31									
		GND					AH32									
		GND					AJ30									
		GND					AJ33									
		GND					AJ34									
		GND					AK31									
		GND					AK32									
		GND					AL33									
		GND					AL34									
		GND					E34									
		GND					F31									
		GND					F32									
		GND					G30									
		GND					G33									
		GND					G34									
		GND					H31									
		GND					H32									
		GND					J30									
		GND					J33									
		GND					J34									
		GND					K31									
		GND					K32									
		GND					L30									
		GND					L33									
		GND					L34									
		GND					M30									
		GND					M31									
		GND					M32									
		GND					N28									
		GND					N29									
		GND					N33									
		GND					N34									
		GND					P27									
		GND					P31									
		GND					P32									
		GND					R28									
		GND					R30									
		GND					R33									
		GND					R34									
		GND					T27									
		GND					T29									
		GND					T31									
		GND					T32									
		GND					U28									
		GND					U33									
		GND					U34									
		GND					V27									
		GND					V31									
		GND					V32									
		GND					W28									
		GND					W30									
		GND					W33									
		GND					W34									
		GND					Y27									
		GND					Y29									
		GND					Y31									
		GND					Y32									
		GND					AA1									
		GND					AA2									
		GND					AB3									
		GND					AB4									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					AJ5									
		GND					AK3									
		GND					AK4									
		GND					AL1									
		GND					AL2									
		GND					AL3									
		GND					AN1									
		GND					V3									
		GND					V4									
		GND					V7									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					R18									
		VCCP					T21									
		VCCP					V25									
		VCCP					W10									
		VCCP					Y10									
		VCCP					Y12									
		VCCP					Y22									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCP					Y24									
		VCCP					Y25									
		VCCA_FPLL					V26									
		VCCA_FPLL					V9									
		VCCA_FPLL					T26									
		VCCPLL_HPS					M9									
		VCCBAT					M27									
		VCC_AUX					AA24									
		VCC_AUX					Y11									
		VCC_AUX					R24									
		VCC_AUX_SHARED					R12									
		VCCD_FPLL					Y26									
		VCCD_FPLL					Y9									
		VCCD_FPLL					P26									
		VCCA_GXBL0					Y28									
		VCCA_GXBR0					Y7									
		VCCA_GXBL1					T28									
		VCCH_GXBL0					V28									
		VCCH_GXBR0					V6									
		VCCH_GXBL1					P28									
		VCCL_GXBL0					V29									
		VCCL_GXBL0					V30									
		VCCL_GXBR0					V5									
		VCCL_GXBR0					Y5									
		VCCL_GXBL1					P29									
		VCCL_GXBL1					P30									
		VCCR_GXBL					AA30									
		VCCR_GXBL					AB29									
		VCCR_GXBL					N30									
		VCCR_GXBL					R29									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AB6									
		VCCR_GXBR					AB5									
		VCCT_GXBL0					T30									
		VCCT_GXBL0					U29									
		VCCT_GXBL0					U30									
		VCCT_GXBR0					W6									
		VCCT_GXBR0					AA6									
		VCCT_GXBL1					W29									
		VCCT_GXBL1					Y30									
		VCC					AA20									
		VCC					T19									
		VCC					T23									
		VCC					T25									
		VCC					V24									
		VCC					U18									
		VCC					U20									
		VCC					U22									
		VCC					U24									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V20									
		VCC					V21									
		VCC					V22									
		VCC					V23									
		VCC					W16									
		VCC					W14									
		VCC					W20									
		VCC					W22									
		VCC					W24									
		VCC					Y13									
		VCC					Y14									
		VCC					Y15									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					Y23									
		VCC					W18									
		VCC_HPS					T11									
		VCC_HPS					U10									
		VCC_HPS					U12									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					W12									
		VCCIO3A					AF27									
		VCCIO3A					AF30									
		VCCIO3A					AH30									
		VCCIO3A					AJ28									
		VCCIO3A					AK30									
		VCCIO3A					AN29									
		VCCIO3B					AF25									
		VCCIO3B					AK24									
		VCCIO3B					AN24									
		VCCIO3C					AD21									
		VCCIO3C					AF21									
		VCCIO3C					AJ21									
		VCCIO3C					AM21									
		VCCIO3D					AE18									
		VCCIO3D					AH18									
		VCCIO3D					AL18									
		VCCIO4A					AD5									
		VCCIO4A					AE8									
		VCCIO4A					AF5									
		VCCIO4A					AH5									
		VCCIO4A					AK5									
		VCCIO4B					AD11									
		VCCIO4B					AF10									
		VCCIO4B					AJ10									
		VCCIO4B					AM9									
		VCCIO4C					AE13									
		VCCIO4C					AH12									
		VCCIO4C					AL12									
		VCCIO4D					AF15									
		VCCIO4D					AJ15									
		VCCIO4D					AM15									
		VCCIO4D					AN17									
		VCCIO6A_HPS					B3									
		VCCIO6A_HPS					C6									
		VCCIO6A_HPS					D3									
		VCCIO6A_HPS					D8									
		VCCIO6A_HPS					E6									
		VCCIO6A_HPS					F2									
		VCCIO6A_HPS					H5									
		VCCIO6A_HPS					H7									
		VCCIO6A_HPS					M7									
		VCCIO6B_HPS					L4									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCIO6B_HPS					M1									
		VCCIO6B_HPS					N8									
		VCCIO6B_HPS					P3									
		VCCIO6B_HPS					R6									
		VCCIO6B_HPS					U5									
		VCCIO6B_HPS					V2									
		VCCIO7A_HPS					B9									
		VCCIO7A_HPS					D11									
		VCCIO7A_HPS					E13									
		VCCIO7A_HPS					K11									
		VCCIO7B_HPS					B13									
		VCCIO7B_HPS					L13									
		VCCIO7C_HPS					H15									
		VCCIO7D_HPS					E17									
		VCCIO7D_HPS					H18									
		VCCIO7E_HPS					L18									
		VCCIO8A					C27									
		VCCIO8A					C30									
		VCCIO8A					E29									
		VCCIO8A					E32									
		VCCIO8A					G27									
		VCCIO8A					K27									
		VCCIO8B					B24									
		VCCIO8B					F24									
		VCCIO8B					J24									
		VCCIO8C					B22									
		VCCIO8C					D21									
		VCCIO8C					G21									
		VCCIO8C					L21									
		VCCIO8D					B18									
		VCCIO8D					B20									
		VCCIO8D					H20									
		VCCPD3					AA21									
		VCCPD3					AA23									
		VCCPD3					AB26									
		VCCPD3					AC28									
		VCCPD4A					AB8									
		VCCPD4BCD					AA11									
		VCCPD4BCD					AA14									
		VCCPD4BCD					AA15									
		VCCPD4BCD					AB9									
		VCCPD6A6B_HPS					P9									
		VCCPD6A6B_HPS					R8									
		VCCPD6A6B_HPS					U7									
		VCCPD6A6B_HPS					U8									
		VCCPD7A_HPS					R11									
		VCCPD7B_HPS					R13									
		VCCPD7C_HPS					T15									
		VCCPD7D_HPS					R16									
		VCCPD7E_HPS					P17									
		VCCPD8					P23									
		VCCPD8					P25									
		VCCPD8					R20									
		VCCPD8					R22									
		VCCPGM					H13									
		VCCPGM					AC29									
		VCCRSTCLK_HPS					H9									
		VCC_HPS					R10									
		VCC_HPS					R14									
		VCC_HPS					T13									
		VCC_HPS					T9									
	VREFB7A7B7C7D7EN0_HPS	VREFB7A7B7C7D7EN0_HPS					P15									
		GND					A19									
		GND					A22									
		GND					A5									
		GND					AA10									
		GND					AA13									
		GND					AA16									
		GND					AA19									
		GND					AA22									
		GND					AA25									
		GND					AA9									
		GND					AB7									
		GND					AC6									
		GND					AD10									
		GND					AD13									
		GND					AD16									
		GND					AD19									
		GND					AD22									
		GND					AD25									
		GND					AD28									
		GND					AD7									
		GND					AG10									
		GND					AG13									
		GND					AG16									
		GND					AG19									
		GND					AG22									
		GND					AG25									
		GND					AG28									
		GND					AG7									
		GND					AK10									
		GND					AK13									
		GND					AK16									
		GND					AK19									
		GND					AK22									
		GND					AK25									
		GND					AK28									
		GND					AK7									
		GND					AN10									
		GND					AN13									
		GND					AN16									
		GND					AN19									
		GND					AN22									
		GND					AN25									
		GND					AN28									
		GND					AN31									
		GND					AN4									
		GND					AN7									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B25									
		GND					B28									
		GND					B31									
		GND					B33									
		GND					B8									
		GND					C19									
		GND					C22									
		GND					C5									
		GND					D2									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					D30									
		GND					E14									
		GND					E25									
		GND					E28									
		GND					E8									
		GND					F19									
		GND					F22									
		GND					F5									
		GND					G11									
		GND					G2									
		GND					H25									
		GND					H28									
		GND					H8									
		GND					J13									
		GND					J19									
		GND					J22									
		GND					J5									
		GND					K16									
		GND					K2									
		GND					L25									
		GND					L28									
		GND					L8									
		GND					M19									
		GND					M22									
		GND					M5									
		GND					N11									
		GND					N15									
		GND					N2									
		GND					N24									
		GND					P13									
		GND					P18									
		GND					P8									
		GND					V18									
		GND					V14									
		GND					V16									
		GND					V8									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					W23									
		GND					W25									
		GND					W9									
		GND					Y18									
		GND					Y20									
		GND					R17									
		GND					R19									
		GND					R21									
		GND					R23									
		GND					R25									
		GND					R5									
		GND					R9									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T2									
		GND					T20									
		GND					T22									
		GND					T24									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U23									
		GND					U25									
		GND					U6									
		GND					U9									
		GND					V10									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the Arria V Device Family Pin Connection Guidelines.
(2) GX8_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
(4) Pins with * are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the Transceiver Clocking in Arria V Devices chapter.
(5) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					A38									
		DNU					B38									
		RREF_TL					B39									
GXB_L2		REFCLK5Ln					U32									
GXB_L2		REFCLK5Lp					U31									
GXB_L2		GXB_TX_L17n					C36									
GXB_L2		GXB_TX_L17p					C37									
GXB_L2		GXB_RX_L17p,GXB_REFCLK_L17p					D39									
GXB_L2		GXB_RX_L17n,GXB_REFCLK_L17n					D38									
GXB_L2		GXB_TX_L16n					E36									
GXB_L2		GXB_TX_L16p					E37									
GXB_L2		GXB_RX_L16p,GXB_REFCLK_L16p					F39									
GXB_L2		GXB_RX_L16n,GXB_REFCLK_L16n					F38									
GXB_L2		GXB_TX_L15n					G36									
GXB_L2		GXB_TX_L15p					G37									
GXB_L2		GXB_RX_L15p,GXB_REFCLK_L15p					H39									
GXB_L2		GXB_RX_L15n,GXB_REFCLK_L15n					H38									
GXB_L2		GXB_TX_L14n					J36									
GXB_L2		GXB_TX_L14p					J37									
GXB_L2		GXB_RX_L14p,GXB_REFCLK_L14p					K39									
GXB_L2		GXB_RX_L14n,GXB_REFCLK_L14n					K38									
GXB_L2		GXB_TX_L13n					L36									
GXB_L2		GXB_TX_L13p					L37									
GXB_L2		GXB_RX_L13p,GXB_REFCLK_L13p					M39									
GXB_L2		GXB_RX_L13n,GXB_REFCLK_L13n					M38									
GXB_L2		GXB_TX_L12n					N36									
GXB_L2		GXB_TX_L12p					N37									
GXB_L2		GXB_RX_L12p,GXB_REFCLK_L12p					P39									
GXB_L2		GXB_RX_L12n,GXB_REFCLK_L12n					P38									
GXB_L2		REFCLK4Ln					W32									
GXB_L2		REFCLK4Lp					W31									
GXB_L1		REFCLK3Ln					AA32									
GXB_L1		REFCLK3Lp					AA31									
GXB_L1		GXB_TX_L11n					R36									
GXB_L1		GXB_TX_L11p					R37									
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					T39									
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					T38									
GXB_L1		GXB_TX_L10n					U36									
GXB_L1		GXB_TX_L10p					U37									
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					V39									
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					V38									
GXB_L1		GXB_TX_L9n					W36									
GXB_L1		GXB_TX_L9p					W37									
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					Y39									
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					Y38									
GXB_L1		GXB_TX_L8n					AA36									
GXB_L1		GXB_TX_L8p					AA37									
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AB39									
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AB38									
GXB_L1		GXB_TX_L7n					AC36									
GXB_L1		GXB_TX_L7p					AC37									
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AD39									
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AD38									
GXB_L1		GXB_TX_L6n					AE36									
GXB_L1		GXB_TX_L6p					AE37									
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AF39									
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AF38									
GXB_L1		REFCLK2Ln					AC32									
GXB_L1		REFCLK2Lp					AC31									
GXB_L0		REFCLK1Ln					AE32									
GXB_L0		REFCLK1Lp					AE31									
GXB_L0		GXB_TX_L5n					AG36									
GXB_L0		GXB_TX_L5p					AG37									
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					AH39									
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					AH38									
GXB_L0		GXB_TX_L4n					AJ36									
GXB_L0		GXB_TX_L4p					AJ37									
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AK39									
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AK38									
GXB_L0		GXB_TX_L3n					AL36									
GXB_L0		GXB_TX_L3p					AL37									
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AM39									
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AM38									
GXB_L0		GXB_TX_L2n					AN36									
GXB_L0		GXB_TX_L2p					AN37									
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AP39									
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AP38									
GXB_L0		GXB_TX_L1n					AR36									
GXB_L0		GXB_TX_L1p					AR37									
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AT39									
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AT38									
GXB_L0		GXB_TX_L0n					AU36									
GXB_L0		GXB_TX_L0p					AU37									
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AW37									
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AW36									
GXB_L0		REFCLK0Ln					AG33									
GXB_L0		REFCLK0Lp					AG32									
		DNU					AH31									
3A		TDO		TDO			AT34									
3A		TMS		TMS			AM35									
3A		TCK		TCK			AV34									
3A		TDI		TDI			AT33									
3A		DCLK		DCLK			AW34									
3A		nCSO		DATA4			AR34									
3A		AS_DATA3		DATA3			AU34									
3A		AS_DATA2		DATA2			AR33									
3A		AS_DATA1		DATA1			AU33									
3A		AS_DATA0,ASDO		DATA0			AV33									
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AN33									
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AP33	DQ1B								
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AN34	DQ1B								
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AP34	DQ1B								
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AK32									
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AL32	DQ1B								
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ34	DQSn1B/QK1B								
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK34	DQS1B/CQ1B/CQn1B/QKn1B								
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AL34									
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AM34	DQ1B								
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AJ33	DQ1B								
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AK33	DQ1B								
3A	VREFB3AN0	IO	VREFB3AN0				AJ31									
3A	VREFB3AN0	IO					AK31	DQ1B								
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AL33	DQ1B								
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AM33	DQ1B								
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AN32				CS# 3A_1	CS# 3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AP32	DQ2B	DQ1B		CS# 3A_0	CS# 3A_0				
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AT32	DQ2B	DQ1B							
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AU32	DQ2B	DQ1B							
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AL31				ODT_3A_1	ODT_3A_1				
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AM31	DQ2B	DQ1B		ODT_3A_0	ODT_3A_0				

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AW33	DQSn2B/QK2B	DQ1B		WE# 3A					
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AW32	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B		CAS# 3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AN31				RAS# 3A					
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AP31	DQ2B	DQ1B		BA 3A 2					
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AR31	DQ2B	DQ1B		BA 3A 1					
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AT31	DQ2B	DQ1B		BA 3A 0					
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AD29				A 3A 15					
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE29	DQ2B	DQ1B		A 3A 14					
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AG30	DQ2B	DQ1B		A 3A 13					
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AH30	DQ2B	DQ1B		A_3A_12					
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AU31				A_3A_11					
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AV31	DQ3B	DQ1B		A_3A_10					
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AW30	DQ3B	DQ1B		A_3A_9	CA_3A_9				
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AW31	DQ3B	DQ1B		A_3A_8	CA_3A_8				
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AK30				A_3A_7	CA_3A_7				
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AL30	DQ3B	DQ1B		A_3A_6	CA_3A_6				
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AR30	DQSn3B/QK3B	DQSn1B/QK1B		A_3A_5	CA_3A_5				
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AT30	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B		A_3A_4	CA_3A_4				
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AU30				A_3A_3	CA_3A_3				
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AV30	DQ3B	DQ1B		A_3A_2	CA_3A_2				
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AT29	DQ3B	DQ1B		A 3A 1	CA_3A_1				
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AU29	DQ3B	DQ1B		A_3A_0	CA_3A_0				
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AN30				CKE 3A 1	CKE 3A 1				
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AP30	DQ3B	DQ1B		CKE 3A 0	CKE 3A 0				
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AN29	DQ3B	DQ1B		CK# 3A	CK# 3A				
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AP29	DQ3B	DQ1B		CK 3A	CK 3A				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AB29				RESET# 3A					
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AC29	DQ4B	DQ2B	DQ1B	DQ1_3B_8	DQ1_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AF28	DQ4B	DQ2B	DQ1B	DQ1_3B_7	DQ1_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AG28	DQ4B	DQ2B	DQ1B	DQ1_3B_6	DQ1_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AK29									
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AL29	DQ4B	DQ2B	DQ1B	DM1_3B	DM1_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AH28	DQSn4B/QK4B	DQ2B	DQ1B	DQS#1_3B	DQS#1_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AJ28	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B	DQS1_3B	DQS1_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AD28									
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AE28	DQ4B	DQ2B	DQ1B	DQ1_3B_5	DQ1_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AB27	DQ4B	DQ2B	DQ1B	DQ1_3B_4	DQ1_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AB28	DQ4B	DQ2B	DQ1B	DQ1_3B_3	DQ1_3B_3				
3B	VREFB3BN0	IO	VREFB3BN0				AL28									
3B	VREFB3BN0	IO					AM28	DQ4B	DQ2B	DQ1B	DQ1_3B_2	DQ1_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AC27	DQ4B	DQ2B	DQ1B	DQ1_3B_1	DQ1_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AD27	DQ4B	DQ2B	DQ1B	DQ1_3B_0	DQ1_3B_0				
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AP28									
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AR28	DQ5B	DQ2B	DQ1B	DQ2_3B_8	DQ2_3B_8				
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AU28	DQ5B	DQ2B	DQ1B	DQ2_3B_7	DQ2_3B_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AV28	DQ5B	DQ2B	DQ1B	DQ2_3B_6	DQ2_3B_6				
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AJ27									
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AK27	DQ5B	DQ2B	DQ1B	DM2_3B	DM2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AW29	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B	DQS#2_3B	DQS#2_3B				
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AW28	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2_3B	DQS2_3B				
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AP27									
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AR27	DQ5B	DQ2B	DQ1B	DQ2_3B_5	DQ2_3B_5				
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AT27	DQ5B	DQ2B	DQ1B	DQ2_3B_4	DQ2_3B_4				
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AU27	DQ5B	DQ2B	DQ1B	DQ2_3B_3	DQ2_3B_3				
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AM27									
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AN27	DQ5B	DQ2B	DQ1B	DQ2_3B_2	DQ2_3B_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AV27	DQ5B	DQ2B	DQ1B	DQ2_3B_1	DQ2_3B_1				
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AW27	DQ5B	DQ2B	DQ1B	DQ2_3B_0	DQ2_3B_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AG27									
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AH27	DQ6B	DQ3B	DQ1B	DQ3_3C_8	DQ3_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AB25	DQ6B	DQ3B	DQ1B	DQ3_3C_7	DQ3_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AC25	DQ6B	DQ3B	DQ1B	DQ3_3C_6	DQ3_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AE27									
3C	VREFB3CN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AF27	DQ6B	DQ3B	DQ1B	DM3_3C	DM3_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AE25	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B	DQS#3_3C	DQS#3_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AF25	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_3C	DQS3_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AC24									
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AD25	DQ6B	DQ3B	DQ1B	DQ3_3C_5	DQ3_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AG26	DQ6B	DQ3B	DQ1B	DQ3_3C_4	DQ3_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AH26	DQ6B	DQ3B	DQ1B	DQ3_3C_3	DQ3_3C_3				
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AD26									
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AE26	DQ6B	DQ3B	DQ1B	DQ3_3C_2	DQ3_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AG25	DQ6B	DQ3B	DQ1B	DQ3_3C_1	DQ3_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AH25	DQ6B	DQ3B	DQ1B	DQ3_3C_0	DQ3_3C_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AN26									
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AP26	DQ7B	DQ3B	DQ1B	DQ4_3C_8	DQ4_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AM25	DQ7B	DQ3B	DQ1B	DQ4_3C_7	DQ4_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AN25	DQ7B	DQ3B	DQ1B	DQ4_3C_6	DQ4_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AJ25									
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AK25	DQ7B	DQ3B	DQ1B	DM4_3C	DM4_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AT26	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B	DQS#4_3C	DQS#4_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AU26	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C	DQS4_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AR25									
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AT25	DQ7B	DQ3B	DQ1B	DQ4_3C_5	DQ4_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AW25	DQ7B	DQ3B	DQ1B	DQ4_3C_4	DQ4_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AW26	DQ7B	DQ3B	DQ1B	DQ4_3C_3	DQ4_3C_3				
3C	VREFB3CN0	IO	VREFB3CN0				AK26									
3C	VREFB3CN0	IO					AL26	DQ7B	DQ3B	DQ1B	DQ4_3C_2	DQ4_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AV25	DQ7B	DQ3B	DQ1B	DQ4_3C_1	DQ4_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AV24	DQ7B	DQ3B	DQ1B	DQ4_3C_0	DQ4_3C_0				
3C	VREFB3CN0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AD23									
3C	VREFB3CN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AD24	DQ8B	DQ4B	DQ2B	DQ5_3C_8	DQ5_3C_8				
3C	VREFB3CN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AT24	DQ8B	DQ4B	DQ2B	DQ5_3C_7	DQ5_3C_7				
3C	VREFB3CN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AU24	DQ8B	DQ4B	DQ2B	DQ5_3C_6	DQ5_3C_6				
3C	VREFB3CN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AK24									
3C	VREFB3CN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AL24	DQ8B	DQ4B	DQ2B	DM5_3C	DM5_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AE24	DQSn8B/QK8B	DQ4B	DQ2B	DQS#5_3C	DQS#5_3C				
3C	VREFB3CN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AF24	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B	DQ2B	DQS5_3C	DQS5_3C				
3C	VREFB3CN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AG24									
3C	VREFB3CN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AH24	DQ8B	DQ4B	DQ2B	DQ5_3C_5	DQ5_3C_5				
3C	VREFB3CN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AW23	DQ8B	DQ4B	DQ2B	DQ5_3C_4	DQ5_3C_4				
3C	VREFB3CN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AW24	DQ8B	DQ4B	DQ2B	DQ5_3C_3	DQ5_3C_3				
3C	VREFB3CN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AN24									
3C	VREFB3CN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AP24	DQ8B	DQ4B	DQ2B	DQ5_3C_2	DQ5_3C_2				
3C	VREFB3CN0	IO			DIFFIO_RX_B61n	DIFFOUT_B61n	AT23	DQ8B	DQ4B	DQ2B	DQ5_3C_1	DQ5_3C_1				
3C	VREFB3CN0	IO			DIFFIO_RX_B61p	DIFFOUT_B61p	AU23	DQ8B	DQ4B	DQ2B	DQ5_3C_0	DQ5_3C_0				
3D	VREFB3DN0	IO			DIFFIO_TX_B62n	DIFFOUT_B62n	AN23									
3D	VREFB3DN0	IO			DIFFIO_TX_B62p	DIFFOUT_B62p	AP23	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	AD22	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	AE23	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AK23									
3D	VREFB3DN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AL23	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B65n	DIFFOUT_B65n	AT22	DQSn9B/QK9B	DQSn4B/QK4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B65p	DIFFOUT_B65p	AU22	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B66n	DIFFOUT_B66n	AV22									
3D	VREFB3DN0	IO			DIFFIO_TX_B66p	DIFFOUT_B66p	AW22	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AV21	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AW21	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AG23									
3D	VREFB3DN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AH23	DQ9B	DQ4B	DQ2B						

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3D	VREFB3DN0	IO			DIFFIO_RX_B69n	DIFFOUT_B69n	AE22	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B69p	DIFFOUT_B69p	AF22	DQ9B	DQ4B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B70n	DIFFOUT_B70n	AN22									
3D	VREFB3DN0	IO			DIFFIO_TX_B70p	DIFFOUT_B70p	AP22	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AW19	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AW20	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK22									
3D	VREFB3DN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AL22	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B73n	DIFFOUT_B73n	AR21	DQSn10B/QK10B	DQ5B	DQSn2B/QK2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B73p	DIFFOUT_B73p	AT21	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B	DQS2B/CQ2B/CQn2B/QKn2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B74n	DIFFOUT_B74n	AG22									
3D	VREFB3DN0	IO			DIFFIO_TX_B74p	DIFFOUT_B74p	AH22	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AT20	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AU20	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	VREFB3DN0				AJ21									
3D	VREFB3DN0	IO					AK21	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AU19	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AV19	DQ10B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AM21									
3D	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AN21	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AE21	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AF21	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AD21									
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AC22	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AG21	DQSn11B/QK11B	DQSn5B/QK5B	DQ2B						
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AH21	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AN20									
3D	VREFB3DN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AP20	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AC21	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AD20	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO			DIFFIO_TX_B83n	DIFFOUT_B83n	AG20									
3D	VREFB3DN0	IO			DIFFIO_TX_B83p	DIFFOUT_B83p	AH20	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AK20	DQ11B	DQ5B	DQ2B						
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AL20	DQ11B	DQ5B	DQ2B						
		VCCD_FPLL					AB20									
		VCCA_FPLL					AB21									
		DNU					AE20									
4D	VREFB4DN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AV18									
4D	VREFB4DN0	IO			DIFFIO_TX_B85p	DIFFOUT_B85p	AW18	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B86n	DIFFOUT_B86n	AG19	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B86p	DIFFOUT_B86p	AH19	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_TX_B87n	DIFFOUT_B87n	AN19									
4D	VREFB4DN0	IO			DIFFIO_TX_B87p	DIFFOUT_B87p	AP19	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B88n	DIFFOUT_B88n	AK19	DQSn12B/QK12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B88p	DIFFOUT_B88p	AL19	DQS12B/CQ12B/CQn12B/QKn12B								
4D	VREFB4DN0	IO			DIFFIO_TX_B89n	DIFFOUT_B89n	AH18									
4D	VREFB4DN0	IO			DIFFIO_TX_B89p	DIFFOUT_B89p	AJ18	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AU18	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AT19	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AE19									
4D	VREFB4DN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AF19	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AW17	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AW16	DQ12B								
4D	VREFB4DN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AK17				CS# 4D 1	CS# 4D 1				
4D	VREFB4DN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AL17	DQ13B	DQ6B		CS# 4D 0	CS# 4D 0				
4D	VREFB4DN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AT17	DQ13B	DQ6B							
4D	VREFB4DN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AU17	DQ13B	DQ6B		A 4D 15					
4D	VREFB4DN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AC19				ODT 4D 1	ODT 4D 1				
4D	VREFB4DN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AD19	DQ13B	DQ6B		ODT 4D 0	ODT 4D 0				
4D	VREFB4DN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AP18	DQSn13B/QK13B	DQ6B		WE# 4D					
4D	VREFB4DN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AR18	DQS13B/CQ13B/CQn13B/QKn13B	DQ6B		CAS# 4D					
4D	VREFB4DN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AD17				RAS# 4D					
4D	VREFB4DN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AC18	DQ13B	DQ6B		BA 4D 2					
4D	VREFB4DN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AD18	DQ13B	DQ6B		BA 4D 1					
4D	VREFB4DN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AE18	DQ13B	DQ6B		BA 4D 0					
4D	VREFB4DN0	IO	VREFB4DN0				AF18									
4D	VREFB4DN0	IO					AG18	DQ13B	DQ6B		A 4D 14					
4D	VREFB4DN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AL18	DQ13B	DQ6B		A 4D 13					
4D	VREFB4DN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AM18	DQ13B	DQ6B		A_4D_12					
4D	VREFB4DN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AG17				A_4D_11					
4D	VREFB4DN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AH17	DQ14B	DQ6B		A 4D 10					
4D	VREFB4DN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AN17	DQ14B	DQ6B		A 4D 9	CA 4D 9				
4D	VREFB4DN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AP17	DQ14B	DQ6B		A 4D 8	CA 4D 8				
4D	VREFB4DN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AR16				A 4D 7	CA 4D 7				
4D	VREFB4DN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AT16	DQ14B	DQ6B		A 4D 6	CA 4D 6				
4D	VREFB4DN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AU16	DQSn14B/QK14B	DQSn6B/QK6B		A 4D 5	CA 4D 5				
4D	VREFB4DN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AV16	DQS14B/CQ14B/CQn14B/QKn14B	DQS6B/CQ6B/CQn6B/QKn6B		A_4D_4	CA_4D_4				
4D	VREFB4DN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AJ16				A_4D_3	CA_4D_3				
4D	VREFB4DN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AK16	DQ14B	DQ6B		A 4D 2	CA 4D 2				
4D	VREFB4DN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AN16	DQ14B	DQ6B		A 4D 1	CA 4D 1				
4D	VREFB4DN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AP16	DQ14B	DQ6B		A 4D 0	CA 4D 0				
4D	VREFB4DN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AL16				CKE 4D 1	CKE 4D 1				
4D	VREFB4DN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AM16	DQ14B	DQ6B		CKE 4D 0	CKE 4D 0				
4D	VREFB4DN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AE17	DQ14B	DQ6B		CK# 4D	CK# 4D				
4D	VREFB4DN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AF16	DQ14B	DQ6B		CK 4D	CK 4D				
4C	VREFB4CN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AN15				RESET# 4D					
4C	VREFB4CN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AP15	DQ15B	DQ7B	DQ3B	DQ1 4C 8	DQ1 4C 8				
4C	VREFB4CN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AW14	DQ15B	DQ7B	DQ3B	DQ1 4C 7	DQ1 4C 7				
4C	VREFB4CN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AW15	DQ15B	DQ7B	DQ3B	DQ1 4C 6	DQ1 4C 6				
4C	VREFB4CN0	IO			DIFFIO_TX_B110n	DIFFOUT_B110n	AC16									
4C	VREFB4CN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AD16	DQ15B	DQ7B	DQ3B	DM1 4C	DM1 4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AG16	DQSn15B/QK15B	DQ7B	DQ3B	DQS#1 4C	DQS#1 4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AH16	DQS15B/CQ15B/CQn15B/QKn15B	DQ7B	DQ3B	DQS1 4C	DQS1 4C				
4C	VREFB4CN0	IO			DIFFIO_TX_B112n	DIFFOUT_B112n	AK15									
4C	VREFB4CN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AL15	DQ15B	DQ7B	DQ3B	DQ1 4C 5	DQ1 4C 5				
4C	VREFB4CN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AV13	DQ15B	DQ7B	DQ3B	DQ1 4C 4	DQ1 4C 4				
4C	VREFB4CN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AW13	DQ15B	DQ7B	DQ3B	DQ1 4C 3	DQ1 4C 3				
4C	VREFB4CN0	IO	VREFB4CN0				AG15									
4C	VREFB4CN0	IO					AH15	DQ15B	DQ7B	DQ3B	DQ1 4C 2	DQ1 4C 2				
4C	VREFB4CN0	IO			DIFFIO_RX_B114n	DIFFOUT_B114n	AT15	DQ15B	DQ7B	DQ3B	DQ1 4C 1	DQ1 4C 1				
4C	VREFB4CN0	IO			DIFFIO_RX_B114p	DIFFOUT_B114p	AU15	DQ15B	DQ7B	DQ3B	DQ1 4C 0	DQ1 4C 0				
4C	VREFB4CN0	IO			DIFFIO_TX_B115n	DIFFOUT_B115n	AC15									
4C	VREFB4CN0	IO			DIFFIO_TX_B115p	DIFFOUT_B115p	AD14	DQ16B	DQ7B	DQ3B	DQ2 4C 8	DQ2 4C 8				
4C	VREFB4CN0	IO			DIFFIO_RX_B116n	DIFFOUT_B116n	AT14	DQ16B	DQ7B	DQ3B	DQ2 4C 7	DQ2 4C 7				
4C	VREFB4CN0	IO			DIFFIO_RX_B116p	DIFFOUT_B116p	AU14	DQ16B	DQ7B	DQ3B	DQ2 4C 6	DQ2 4C 6				
4C	VREFB4CN0	IO			DIFFIO_TX_B117n	DIFFOUT_B117n	AT13									
4C	VREFB4CN0	IO			DIFFIO_TX_B117p	DIFFOUT_B117p	AU13	DQ16B	DQ7B	DQ3B	DM2 4C	DM2 4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B118n	DIFFOUT_B118n	AE16	DQSn16B/QK16B	DQSn7B/QK7B	DQ3B	DQS#2 4C	DQS#2 4C				
4C	VREFB4CN0	IO			DIFFIO_RX_B118p	DIFFOUT_B118p	AF15	DQS16B/CQ16B/CQn16B/QKn16B	DQS7B/CQ7B/CQn7B/QKn7B	DQ3B	DQS2 4C	DQS2 4C				
4C	VREFB4CN0	IO			DIFFIO_TX_B119n	DIFFOUT_B119n	AK14									
4C	VREFB4CN0	IO			DIFFIO_TX_B119p	DIFFOUT_B119p	AL14	DQ16B	DQ7B	DQ3B	DQ2 4C 5	DQ2 4C 5				
4C	VREFB4CN0	IO			DIFFIO_RX_B120n	DIFFOUT_B120n	AN14	DQ16B	DQ7B	DQ3B	DQ2 4C 4	DQ2 4C 4				
4C	VREFB4CN0	IO			DIFFIO_RX_B120p	DIFFOUT_B120p	AP14	DQ16B	DQ7B	DQ3B	DQ2 4C 3	DQ2 4C 3				
4C	VREFB4CN0	IO			DIFFIO_TX_B121n	DIFFOUT_B121n	AG14									
4C	VREFB4CN0	IO			DIFFIO_TX_B121p	DIFFOUT_B121p	AH14	DQ16B	DQ7B	DQ3B	DQ2 4C 2	DQ2 4C 2				
4C	VREFB4CN0	IO			DIFFIO_RX_B122n	DIFFOUT_B122n	AD15	DQ16B	DQ7B	DQ3B	DQ2 4C 1	DQ2 4C 1				
4C	VREFB4CN0	IO			DIFFIO_RX_B122p	DIFFOUT_B122p	AE15	DQ16B	DQ7B	DQ3B	DQ2 4C 0	DQ2 4C 0				
4B	VREFB4BN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AP13									
4B	VREFB4BN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AR13	DQ17B	DQ8B	DQ3B	DQ3_4B_8	DQ3_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B124n	DIFFOUT_B124n	AE14	DQ17B	DQ8B	DQ3B	DQ3_4B_7	DQ3_4B_7				

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4B	VREFB4BN0	IO			DIFFIO_RX_B124p	DIFFOUT_B124p	AE13	DQ17B	DQ8B	DQ3B	DQ3_4B_6	DQ3_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AT12									
4B	VREFB4BN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AU12	DQ17B	DQ8B	DQ3B	DM3_4B	DM3_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B126n	DIFFOUT_B126n	AV12	DQSn17B/QK17B	DQ8B	DQSn3B/QK3B	DQSn3_4B	DQSn3_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B126p	DIFFOUT_B126p	AW12	DQS17B/CQ17B/CQn17B/QKn17B	DQ8B	DQS3B/CQ3B/CQn3B/QKn3B	DQS3_4B	DQS3_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AL13									
4B	VREFB4BN0	IO			DIFFIO_TX_B127p	DIFFOUT_B127p	AM13	DQ17B	DQ8B	DQ3B	DQ3_4B_5	DQ3_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B128n	DIFFOUT_B128n	AW10	DQ17B	DQ8B	DQ3B	DQ3_4B_4	DQ3_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B128p	DIFFOUT_B128p	AW11	DQ17B	DQ8B	DQ3B	DQ3_4B_3	DQ3_4B_3				
4B	VREFB4BN0	IO			DIFFIO_TX_B129n	DIFFOUT_B129n	AN12									
4B	VREFB4BN0	IO			DIFFIO_TX_B129p	DIFFOUT_B129p	AP12	DQ17B	DQ8B	DQ3B	DQ3_4B_2	DQ3_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B130n	DIFFOUT_B130n	AH13	DQ17B	DQ8B	DQ3B	DQ3_4B_1	DQ3_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B130p	DIFFOUT_B130p	AJ13	DQ17B	DQ8B	DQ3B	DQ3_4B_0	DQ3_4B_0				
4B	VREFB4BN0	IO			DIFFIO_TX_B131n	DIFFOUT_B131n	AH12									
4B	VREFB4BN0	IO			DIFFIO_TX_B131p	DIFFOUT_B131p	AJ12	DQ18B	DQ8B	DQ3B	DQ4_4B_8	DQ4_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B132n	DIFFOUT_B132n	AF13	DQ18B	DQ8B	DQ3B	DQ4_4B_7	DQ4_4B_7				
4B	VREFB4BN0	IO			DIFFIO_RX_B132p	DIFFOUT_B132p	AG13	DQ18B	DQ8B	DQ3B	DQ4_4B_6	DQ4_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B133n	DIFFOUT_B133n	AU10									
4B	VREFB4BN0	IO			DIFFIO_TX_B133p	DIFFOUT_B133p	AV10	DQ18B	DQ8B	DQ3B	DM4_4B	DM4_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B134n	DIFFOUT_B134n	AT11	DQSn18B/QK18B	DQSn8B/QK8B	DQ3B	DQS#4_4B	DQS#4_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B134p	DIFFOUT_B134p	AU11	DQS18B/CQ18B/CQn18B/QKn18B	DQS8B/CQ8B/CQn8B/QKn8B	DQ3B	DQS4_4B	DQS4_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B135n	DIFFOUT_B135n	AK12									
4B	VREFB4BN0	IO			DIFFIO_TX_B135p	DIFFOUT_B135p	AL12	DQ18B	DQ8B	DQ3B	DQ4_4B_5	DQ4_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B136n	DIFFOUT_B136n	AC13	DQ18B	DQ8B	DQ3B	DQ4_4B_4	DQ4_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B136p	DIFFOUT_B136p	AD13	DQ18B	DQ8B	DQ3B	DQ4_4B_3	DQ4_4B_3				
4B	VREFB4BN0	IO	VREFB4BN0				AN11									
4B	VREFB4BN0	IO					AP11	DQ18B	DQ8B	DQ3B	DQ4_4B_2	DQ4_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AV9	DQ18B	DQ8B	DQ3B	DQ4_4B_1	DQ4_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AW9	DQ18B	DQ8B	DQ3B	DQ4_4B_0	DQ4_4B_0				
4B	VREFB4BN0	IO			DIFFIO_TX_B138n	DIFFOUT_B138n	AC12									
4B	VREFB4BN0	IO			DIFFIO_TX_B138p	DIFFOUT_B138p	AD11	DQ19B	DQ9B	DQ4B	DQ5_4B_8	DQ5_4B_8				
4B	VREFB4BN0	IO			DIFFIO_RX_B139n	DIFFOUT_B139n	AF12	DQ19B	DQ9B	DQ4B	DQ5_4B_7	DQ5_4B_7				
4B	VREFB4BN0	IO			DIFFIO_RX_B139p	DIFFOUT_B139p	AG12	DQ19B	DQ9B	DQ4B	DQ5_4B_6	DQ5_4B_6				
4B	VREFB4BN0	IO			DIFFIO_TX_B140n	DIFFOUT_B140n	AT9									
4B	VREFB4BN0	IO			DIFFIO_TX_B140p	DIFFOUT_B140p	AU9	DQ19B	DQ9B	DQ4B	DM5_4B	DM5_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B141n	DIFFOUT_B141n	AG11	DQSn19B/QK19B	DQ9B	DQ4B	DQS#5_4B	DQS#5_4B				
4B	VREFB4BN0	IO			DIFFIO_RX_B141p	DIFFOUT_B141p	AH11	DQS19B/CQ19B/CQn19B/QKn19B	DQ9B	DQ4B	DQS5_4B	DQS5_4B				
4B	VREFB4BN0	IO			DIFFIO_TX_B142n	DIFFOUT_B142n	AD12									
4B	VREFB4BN0	IO			DIFFIO_TX_B142p	DIFFOUT_B142p	AE12	DQ19B	DQ9B	DQ4B	DQ5_4B_5	DQ5_4B_5				
4B	VREFB4BN0	IO			DIFFIO_RX_B143n	DIFFOUT_B143n	AP10	DQ19B	DQ9B	DQ4B	DQ5_4B_4	DQ5_4B_4				
4B	VREFB4BN0	IO			DIFFIO_RX_B143p	DIFFOUT_B143p	AR10	DQ19B	DQ9B	DQ4B	DQ5_4B_3	DQ5_4B_3				
4B	VREFB4BN0	IO			DIFFIO_TX_B144n	DIFFOUT_B144n	AK11									
4B	VREFB4BN0	IO			DIFFIO_TX_B144p	DIFFOUT_B144p	AL11	DQ19B	DQ9B	DQ4B	DQ5_4B_2	DQ5_4B_2				
4B	VREFB4BN0	IO			DIFFIO_RX_B145n	DIFFOUT_B145n	AL10	DQ19B	DQ9B	DQ4B	DQ5_4B_1	DQ5_4B_1				
4B	VREFB4BN0	IO			DIFFIO_RX_B145p	DIFFOUT_B145p	AM10	DQ19B	DQ9B	DQ4B	DQ5_4B_0	DQ5_4B_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B146n	DIFFOUT_B146n	AL9									
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B146p	DIFFOUT_B146p	AM9	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA11	DIFFIO_RX_B147n	DIFFOUT_B147n	AW7	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B147p	DIFFOUT_B147p	AW8	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_TX_B148n	DIFFOUT_B148n	AV7									
4A	VREFB4AN0	IO		DATA6	DIFFIO_TX_B148p	DIFFOUT_B148p	AV6	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA12	DIFFIO_RX_B149n	DIFFOUT_B149n	AW6	DQSn20B/QK20B	DQSn9B/QK9B	DQ4B						
4A	VREFB4AN0	IO		DATA13	DIFFIO_RX_B149p	DIFFOUT_B149p	AW5	DQS20B/CQ20B/CQn20B/QKn20B	DQS9B/CQ9B/CQn9B/QKn9B	DQ4B						
4A	VREFB4AN0	IO		DATA7	DIFFIO_TX_B150n	DIFFOUT_B150n	AK9									
4A	VREFB4AN0	IO		DATA8	DIFFIO_TX_B150p	DIFFOUT_B150p	AK10	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA14	DIFFIO_RX_B151n	DIFFOUT_B151n	AU7	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA15	DIFFIO_RX_B151p	DIFFOUT_B151p	AU8	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		DATA9	DIFFIO_TX_B152n	DIFFOUT_B152n	AM9									
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_TX_B152p	DIFFOUT_B152p	AP9	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AT8	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	AR9	DQ20B	DQ9B	DQ4B						
4A	VREFB4AN0	IO		PR_ERROR	DIFFIO_TX_B154n	DIFFOUT_B154n	AH10									
4A	VREFB4AN0	IO		PR_READY	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ10	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		PR_DONE	DIFFIO_RX_B155n	DIFFOUT_B155n	AF10	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		PR_REQUEST	DIFFIO_RX_B155p	DIFFOUT_B155p	AE11	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		nPERSTR0	DIFFIO_TX_B156n	DIFFOUT_B156n	AK6									
4A	VREFB4AN0	IO		nPERSTL0	DIFFIO_TX_B156p	DIFFOUT_B156p	AL6	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		CvP_CONFDONE	DIFFIO_RX_B157n	DIFFOUT_B157n	AH6	DQSn21B/QK21B	DQ10B	DQSn4B/QK4B						
4A	VREFB4AN0	IO		CRC_ERROR	DIFFIO_RX_B157p	DIFFOUT_B157p	AJ6	DQS21B/CQ21B/CQn21B/QKn21B	DQ10B	DQS4B/CQ4B/CQn4B/QKn4B						
4A	VREFB4AN0	IO		DEV_OE	DIFFIO_TX_B158n	DIFFOUT_B158n	AH9									
4A	VREFB4AN0	IO		DEV_CLRn	DIFFIO_TX_B158p	DIFFOUT_B158p	AJ9	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		INIT_DONE	DIFFIO_RX_B159n	DIFFOUT_B159n	AM6	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO		nCEO	DIFFIO_RX_B159p	DIFFOUT_B159p	AN6	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	VREFB4AN0				AH7									
4A	VREFB4AN0	IO					AH8	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AJ7	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AK7	DQ21B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AL7									
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AM7	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AN8	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT_B162p	AP8	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_TX_B163n	DIFFOUT_B163n	AT6									
4A	VREFB4AN0	IO			DIFFIO_TX_B163p	DIFFOUT_B163p	AU6	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AR7	DQSn22B/QK22B	DQSn10B/QK10B	DQ4B						
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AT7	DQS22B/CQ22B/CQn22B/QKn22B	DQS10B/CQ10B/CQn10B/QKn10B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_TX_B165n	DIFFOUT_B165n	AK8									
4A	VREFB4AN0	IO			DIFFIO_TX_B165p	DIFFOUT_B165p	AL8	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B166n	DIFFOUT_B166n	AV4	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AW4	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AN7									
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AP7	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AP6	DQ22B	DQ10B	DQ4B						
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AR6	DQ22B	DQ10B	DQ4B						
		RREF_BR					AW2									
		DNU					AV3									
		DNU					AW3									
GXB_R0		REFCLK0Rp					AF8									
GXB_R0		REFCLK0Rn					AF7									
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AU2									
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AU1									
GXB_R0		GXB_TX_R0p					AT3									
GXB_R0		GXB_TX_R0n					AT4									
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AR2									
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AR1									
GXB_R0		GXB_TX_R1p					AP3									
GXB_R0		GXB_TX_R1n					AP4									
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AN2									
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AN1									
GXB_R0		GXB_TX_R2p					AM3									
GXB_R0		GXB_TX_R2n					AM4									
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AL2									
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AL1									
GXB_R0		GXB_TX_R3p					AK3									
GXB_R0		GXB_TX_R3n					AK4									
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AJ2									
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AJ1									
GXB_R0		GXB_TX_R4p					AH3									
GXB_R0		GXB_TX_R4n					AH4									
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					AG2									
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					AG1									

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
GXB_R0		GXB_TX_R5p					AF3									
GXB_R0		GXB_TX_R5n					AF4									
GXB_R0		REFCLK1Rp					AD9									
GXB_R0		REFCLK1Rn					AD8									
GXB_R1		REFCLK2Rp					AB9									
GXB_R1		REFCLK2Rn					AB8									
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AE2									
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					AE1									
GXB_R1		GXB_TX_R6p					AD3									
GXB_R1		GXB_TX_R6n					AD4									
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AC2									
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AC1									
GXB_R1		GXB_TX_R7p					AB3									
GXB_R1		GXB_TX_R7n					AB4									
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					AA2									
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AA1									
GXB_R1		GXB_TX_R8p					Y3									
GXB_R1		GXB_TX_R8n					Y4									
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					W2									
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					W1									
GXB_R1		GXB_TX_R9p					V3									
GXB_R1		GXB_TX_R9n					V4									
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					U2									
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					U1									
GXB_R1		GXB_TX_R10p					T3									
GXB_R1		GXB_TX_R10n					T4									
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					R2									
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					R1									
GXB_R1		GXB_TX_R11p					P3									
GXB_R1		GXB_TX_R11n					P4									
GXB_R1		REFCLK3Rp					Y9									
GXB_R1		REFCLK3Rn					Y8									
6B	VREFB6BN0_HPS	HPS_DDR					T7				HPS_DM_4	HPS_DM_4				
6B	VREFB6BN0_HPS	HPS_DDR					R6				HPS_DQ_39	HPS_DQ_39				
6B	VREFB6BN0_HPS	HPS_DDR					M1				HPS_DQ_37	HPS_DQ_37				
6B	VREFB6BN0_HPS	HPS_DDR					N1				HPS_DQ_38	HPS_DQ_38				
6B	VREFB6BN0_HPS	HPS_DDR					M2				HPS_DQ_36	HPS_DQ_36				
6B	VREFB6BN0_HPS	HPS_DDR					J1				HPS_DQS_4	HPS_DQS_4				
6B	VREFB6BN0_HPS	HPS_GPI13					K1									
6B	VREFB6BN0_HPS	HPS_DDR					H1				HPS_DQS#_4	HPS_DQS#_4				
6B	VREFB6BN0_HPS	HPS_DDR					L1				HPS_DQ_35	HPS_DQ_35				
6B	VREFB6BN0_HPS	HPS_DDR					F1				HPS_DQ_33	HPS_DQ_33				
6B	VREFB6BN0_HPS	HPS_DDR					P6				HPS_DQ_34	HPS_DQ_34				
6B	VREFB6BN0_HPS	HPS_DDR					G1				HPS_DQ_32	HPS_DQ_32				
6B	VREFB6BN0_HPS	HPS_GPI12					R7									
6B	VREFB6BN0_HPS	HPS_GPI11					J2									
6B	VREFB6BN0_HPS	HPS_DDR					D1				HPS_DM_3	HPS_DM_3				
6B	VREFB6BN0_HPS	HPS_GPI10					K2									
6B	VREFB6BN0_HPS	HPS_DDR					E1				HPS_DQ_31	HPS_DQ_31				
6B	VREFB6BN0_HPS	HPS_DDR					F2				HPS_DQ_29	HPS_DQ_29				
6B	VREFB6BN0_HPS	HPS_DDR					M3				HPS_DQ_30	HPS_DQ_30				
6B	VREFB6BN0_HPS	HPS_DDR					G2				HPS_DQ_28	HPS_DQ_28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					M4									
6B	VREFB6BN0_HPS	HPS_DDR					C2				HPS_DQS_3	HPS_DQS_3				
6B	VREFB6BN0_HPS	HPS_GPI9					B1									
6B	VREFB6BN0_HPS	HPS_DDR					D2				HPS_DQS#_3	HPS_DQS#_3				
6B	VREFB6BN0_HPS	HPS_DDR					C1				HPS_DQ_27	HPS_DQ_27				
6B	VREFB6BN0_HPS	HPS_DDR					A3				HPS_DQ_25	HPS_DQ_25				
6B	VREFB6BN0_HPS	HPS_DDR					P7				HPS_DQ_26	HPS_DQ_26				
6B	VREFB6BN0_HPS	HPS_DDR					A2				HPS_DQ_24	HPS_DQ_24				
6B	VREFB6BN0_HPS	HPS_GPI8					N6									
6B	VREFB6BN0_HPS	HPS_GPI7					K3									
6B	VREFB6BN0_HPS	HPS_DDR					D3				HPS_DM_2	HPS_DM_2				
6B	VREFB6BN0_HPS	HPS_GPI6					K4									
6B	VREFB6BN0_HPS	HPS_DDR					C3				HPS_DQ_23	HPS_DQ_23				
6B	VREFB6BN0_HPS	HPS_DDR					J4				HPS_DQ_21	HPS_DQ_21				
6B	VREFB6BN0_HPS	HPS_DDR					M5				HPS_DQ_22	HPS_DQ_22				
6B	VREFB6BN0_HPS	HPS_DDR					H3				HPS_DQ_20	HPS_DQ_20				
6B	VREFB6BN0_HPS	HPS_GPI5					L4									
6B	VREFB6BN0_HPS	HPS_DDR					G4				HPS_DQS_2	HPS_DQS_2				
6B	VREFB6BN0_HPS	HPS_DDR					E3				HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					H4				HPS_DQS#_2	HPS_DQS#_2				
6B	VREFB6BN0_HPS	HPS_DDR					F3				HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					K5				HPS_DQ_17	HPS_DQ_17				
6B	VREFB6BN0_HPS	HPS_DDR					N7				HPS_DQ_18	HPS_DQ_18				
6B	VREFB6BN0_HPS	HPS_DDR					J5				HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0_HPS	HPS_GPI4					M6									
6A	VREFB6AN0_HPS	HPS_GPI3					C4									
6A	VREFB6AN0_HPS	HPS_DDR					E4				HPS_DM_1	HPS_DM_1				
6A	VREFB6AN0_HPS	HPS_GPI2					B4									
6A	VREFB6AN0_HPS	HPS_DDR					F4				HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					A5				HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					R9				HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					A4				HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					R8				HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					D5				HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					F5				HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					E6				HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					G5				HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					G6				HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					N8				HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					H6				HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_GPI1					M7									
6A	VREFB6AN0_HPS	HPS_GPI0					B6									
6A	VREFB6AN0_HPS	HPS_DDR					C6				HPS_DM_0	HPS_DM_0				
6A	VREFB6AN0_HPS	HPS_DDR					D6				HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					A7				HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					L6				HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					A6				HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					K6				HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					F7				HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0_HPS	HPS_DDR					H7				HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					E7				HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					G7				HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					C7				HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					R10				HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					D7				HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					P10									
6A	VREFB6AN0_HPS	HPS_DDR					N9				HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					M9				HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					A8				HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					N10				HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					B7				HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					M10				HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					A11				HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					B9				HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					B10				HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					A9				HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					C9				HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					L7				HPS_BA_0					

Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB6AN0_HPS	HPS_DDR					D8				HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					G9				HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					G8				HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					D9				HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					K7				HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					C10				HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					J7				HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					H9				HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					F9				HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					J9				HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					E9				HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					D11				HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					J8				HPS_WE#					
6A	VREFB6AN0_HPS	HPS_DDR					D10				HPS_A_15					
6A	VREFB6AN0_HPS	HPS_RZQ_0					K9									
		DNU					B12									
		GND					C11									
		GND					A12									
7A		HPS_nRST					R11									
7A		HPS_nPOR					K10									
7A		HPS_TDO					T11									
		VCCRSTCLK_HPS					J10									
7A		HPS_TMS					F10									
7A		HPS_TCK					G10									
7A		HPS_TRST					F11									
7A		HPS_TDI					H10									
		GND					M11									
7A		HPS_PORSEL					C12									
7A		HPS_CLK1					N11									
7A		HPS_CLK2					D12									
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_CLK					J11						TRACE_CLK			HPS_GPIO48
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D0					K12						TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D1					K11						TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D2					J12						TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D3					H12						TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D4					E12						TRACE_D4	SPIS1_CLK		HPS_GPIO53
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D5					G11						TRACE_D5	SPIS1_MOSI		HPS_GPIO54
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D6					F12						TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A7B7C7D7EN0_HPS	TRACE_D7					A13						TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_CLK					P12						SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MOSI					A14						SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_MISO					N12						SPIM0_MISO		UART1_CTS	HPS_GPIO59
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0,BOOTSEL0					B15						SPIM0_SS0		UART1_RTS	HPS_GPIO60
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX					B14						UART0_RX		SPIM0_SS1	HPS_GPIO61
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX,CLKSEL1					A15						UART0_TX		SPIM1_SS1	HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SDA					C13						I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C0_SCL					L13						I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	UART0_RX*					M12							UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	UART0_TX*,CLKSEL0					M13							UART0_TX	SPIM1_SS0	HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_CLK					L12						SPIS1_CLK	SPIM1_CLK		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MOSI					E13						SPIS1_MOSI	SPIM1_MOSI		HPS_GPIO68
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_MISO					F13						SPIS1_MISO	SPIM1_MISO		HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS1_SS0					D13						SPIS1_SS0	SPIM1_SS0		HPS_GPIO70
7A	VREFB7A7B7C7D7EN0_HPS	UART1_RX					G13						UART1_RX	SPIM1_SS1		HPS_GPIO62
7A	VREFB7A7B7C7D7EN0_HPS	UART1_TX					N13						UART1_TX	SPIM0_CLK		HPS_GPIO63
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SDA					R13						I2C1_SDA	SPIM0_MOSI		HPS_GPIO64
7A	VREFB7A7B7C7D7EN0_HPS	I2C1_SCL					M14						I2C1_SCL	SPIM0_MISO		HPS_GPIO65
7A	VREFB7A7B7C7D7EN0_HPS	SPIM0_SS0					P13							SPIM0_SS0		HPS_GPIO66
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_CLK					H13						SPIS0_CLK	SPIM0_SS1		HPS_GPIO67
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MOSI					C14						SPIS0_MOSI			HPS_GPIO68
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_MISO					J13						SPIS0_MISO			HPS_GPIO69
7A	VREFB7A7B7C7D7EN0_HPS	SPIS0_SS0					D14						SPIS0_SS0			HPS_GPIO70
7B	VREFB7A7B7C7D7EN0_HPS	NAND_ALE					A16						NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CE					P15						NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A7B7C7D7EN0_HPS	NAND_CLE					A17						NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RE					R15						NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A7B7C7D7EN0_HPS	NAND_RB					C16						NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ0					G14						NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ1					B17						NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ2					H14						NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ3					L15						NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ4					P14						NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ5					K15						NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ6					R14						NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A7B7C7D7EN0_HPS	NAND_DQ7					K14						NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WP					C15						NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A7B7C7D7EN0_HPS	NAND_WE,BOOTSEL2					L14						NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO0					D15						QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO1					G15						QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO2					M15						QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_IO3					H15						QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS0,BOOTSEL1					N15						QSPI_SS0			HPS_GPIO33
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_CLK					F15						QSPI_CLK			HPS_GPIO34
7B	VREFB7A7B7C7D7EN0_HPS	QSPI_SS1					E15						QSPI_SS1			HPS_GPIO35
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CMD					D16						SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_PWREN					P16						SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D0					C17						SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D1					N16						SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D4					F16						SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D5					G16						SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D6					E16						SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D7					H16						SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A7B7C7D7EN0_HPS	HPS_GPIO44					K16							USB0_CLK		HPS_GPIO44
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_CCLK_OUT					L16						SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D2					J16						SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A7B7C7D7EN0_HPS	SDMMC_D3					M16						SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CLK					R17						RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD0					F17						RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD1					P17						RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD2					F18						RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TXD3					E18						RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD0					J17						RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDIO					B18						RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_MDC					K17						RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CTL					B19						RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_TX_CTL					A18						RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RX_CLK					C18						RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD1					A19						RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD2					C19						RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A7B7C7D7EN0_HPS	RGMII0_RXD3					G18						RGMII0_RXD3	USB1_NXT		HPS_GPIO13
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CLK					D19						RGMII1_TX_CLK			HPS_GPIO48
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD0					H18						RGMII1_TXD0			HPS_GPIO49
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD1					F19						RGMII1_TXD1			HPS_GPIO50
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_TX_CTL					N18						RGMII1_TX_CTL			HPS_GPIO51
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD0					E19						RGMII1_RXD0			HPS_GPIO52
7D	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD1					M17						RGMII1_RXD1			HPS_GPIO53
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDIO					J18						RGMII1_MDIO	SPIM0_CLK	SPIS0_CLK	HPS_GPIO54
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_MDC					L18						RGMII1_MDC	SPIM0_MOSI	SPIS0_MOSI	HPS_GPIO55
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD2					K18						RGMII1_TXD2	SPIM0_MISO	SPIS0_MISO	HPS_GPIO56
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_TXD3					M18						RGMII1_TXD3	SPIM0_SS0	SPIS0_SS0	HPS_GPIO57

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CLK					G21						RGMII1_RX_CLK	SPIS1_CLK	SPIM1_CLK	HPS_GPIO58
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RX_CTL					H19						RGMII1_RX_CTL	SPIS1_MOSI	SPIM1_MOSI	HPS_GPIO59
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD2					G20						RGMII1_RXD2	SPIS1_MISO	SPIM1_MISO	HPS_GPIO60
7E	VREFB7A7B7C7D7EN0_HPS	RGMII1_RXD3					G19						RGMII1_RXD3	SPIS1_SS0	SPIM1_SS0	HPS_GPIO61
7G	VREFB7GN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	R19									
7G	VREFB7GN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	T19									
7G	VREFB7GN0	IO					N19									
7G	VREFB7GN0	IO	VREFB7GN0				P19									
7G	VREFB7GN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	U19									
7G	VREFB7GN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	U20									
7G	VREFB7GN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	L19									
7G	VREFB7GN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	P20									
7G	VREFB7GN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	R20									
7G	VREFB7GN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	M19									
7G	VREFB7GN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L20									
7G	VREFB7GN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	M20									
		VCCA_FPLL					V20									
		VCCD_FPLL					V19									
		DNU					F20									
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T31p	DIFFOUT_T31p	C20	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T31n	DIFFOUT_T31n	D20	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	N21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	P21									
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T33p	DIFFOUT_T33p	H21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T33n	DIFFOUT_T33n	J21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	D21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	E21									
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T35p	DIFFOUT_T35p	A20	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T						
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T35n	DIFFOUT_T35n	B21	DQSn1T/QK1T	DQSn1T/QK1T	DQ1T						
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T36p	DIFFOUT_T36p	K21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T36n	DIFFOUT_T36n	L21									
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T37p	DIFFOUT_T37p	A22	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T37n	DIFFOUT_T37n	A21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	R21	DQ1T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	T21									
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T39p	DIFFOUT_T39p	B22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T39n	DIFFOUT_T39n	C22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO					J22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO	VREFB8DN0				H22									
8D	VREFB8DN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	E22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	F22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	A23	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	A24									
8D	VREFB8DN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	C23	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS1T/CQ1T/CQn1T/QKn1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	D23	DQSn2T/QK2T	DQ1T	DQSn1T/QK1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	L22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	M22									
8D	VREFB8DN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	N22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	P22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	R22	DQ2T	DQ1T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	T22									
8D	VREFB8DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	F23	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	G23	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	R23	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	T23									
8D	VREFB8DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	B24	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	C24	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	M23	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	N23									
8D	VREFB8DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	D24	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	E24	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	J23	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	K23									
8D	VREFB8DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	F24	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	G24	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	H24	DQ3T	DQ2T	DQ1T						
8D	VREFB8DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	J24									
8C	VREFB8CN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	T26	DQ4T	DQ2T	DQ1T	DQ5_8C_0	DQ5_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	T25	DQ4T	DQ2T	DQ1T	DQ5_8C_1	DQ5_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	G25	DQ4T	DQ2T	DQ1T	DQ5_8C_2	DQ5_8C_2				
8C	VREFB8CN0	IO			DIFFIO_TX_T55n	DIFFOUT_T55n	H25									
8C	VREFB8CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	N24	DQ4T	DQ2T	DQ1T	DQ5_8C_3	DQ5_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	P24	DQ4T	DQ2T	DQ1T	DQ5_8C_4	DQ5_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	R24	DQ4T	DQ2T	DQ1T	DQ5_8C_5	DQ5_8C_5				
8C	VREFB8CN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	T24									
8C	VREFB8CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	A25	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQ1T	DQS5_8C	DQS5_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	B25	DQSn4T/QK4T	DQ2T	DQ1T	DQS#5_8C	DQS#5_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	K24	DQ4T	DQ2T	DQ1T	DM5_8C	DM5_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	L24									
8C	VREFB8CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	D25	DQ4T	DQ2T	DQ1T	DQ5_8C_6	DQ5_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	E25	DQ4T	DQ2T	DQ1T	DQ5_8C_7	DQ5_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	P25	DQ4T	DQ2T	DQ1T	DQ5_8C_8	DQ5_8C_8				
8C	VREFB8CN0	IO			DIFFIO_TX_T61n	DIFFOUT_T61n	R25									
8C	VREFB8CN0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	C26	DQ5T	DQ3T	DQ2T	DQ4_8C_0	DQ4_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	D26	DQ5T	DQ3T	DQ2T	DQ4_8C_1	DQ4_8C_1				
8C	VREFB8CN0	IO					K25	DQ5T	DQ3T	DQ2T	DQ4_8C_2	DQ4_8C_2				
8C	VREFB8CN0	IO	VREFB8CN0				L25									
8C	VREFB8CN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	R26	DQ5T	DQ3T	DQ2T	DQ4_8C_3	DQ4_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	T27	DQ5T	DQ3T	DQ2T	DQ4_8C_4	DQ4_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	A26	DQ5T	DQ3T	DQ2T	DQ4_8C_5	DQ4_8C_5				
8C	VREFB8CN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	A27									
8C	VREFB8CN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	M26	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ2T	DQS4_8C	DQS4_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	N26	DQSn5T/QK5T	DQSn3T/QK3T	DQ2T	DQS#4_8C	DQS#4_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	J26	DQ5T	DQ3T	DQ2T	DM4_8C	DM4_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T66n	DIFFOUT_T66n	K26									
8C	VREFB8CN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	F26	DQ5T	DQ3T	DQ2T	DQ4_8C_6	DQ4_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	G26	DQ5T	DQ3T	DQ2T	DQ4_8C_7	DQ4_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	M25	DQ5T	DQ3T	DQ2T	DQ4_8C_8	DQ4_8C_8				
8C	VREFB8CN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	N25									
8C	VREFB8CN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	P27	DQ6T	DQ3T	DQ2T	DQ3_8C_0	DQ3_8C_0				
8C	VREFB8CN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	R27	DQ6T	DQ3T	DQ2T	DQ3_8C_1	DQ3_8C_1				
8C	VREFB8CN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	H27	DQ6T	DQ3T	DQ2T	DQ3_8C_2	DQ3_8C_2				
8C	VREFB8CN0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	J27									
8C	VREFB8CN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	B27	DQ6T	DQ3T	DQ2T	DQ3_8C_3	DQ3_8C_3				
8C	VREFB8CN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	C27	DQ6T	DQ3T	DQ2T	DQ3_8C_4	DQ3_8C_4				
8C	VREFB8CN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	E27	DQ6T	DQ3T	DQ2T	DQ3_8C_5	DQ3_8C_5				
8C	VREFB8CN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	F27									
8C	VREFB8CN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	R28	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQS2T/CQ2T/CQn2T/QKn2T	DQS3_8C	DQS3_8C				
8C	VREFB8CN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	T28	DQSn6T/QK6T	DQ3T	DQSn2T/QK2T	DQS#3_8C	DQS#3_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	K27	DQ6T	DQ3T	DQ2T	DM3_8C	DM3_8C				
8C	VREFB8CN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	L27									
8C	VREFB8CN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	M27	DQ6T	DQ3T	DQ2T	DQ3_8C_6	DQ3_8C_6				
8C	VREFB8CN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	N27	DQ6T	DQ3T	DQ2T	DQ3_8C_7	DQ3_8C_7				
8C	VREFB8CN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	N28	DQ6T	DQ3T	DQ2T	DQ3_8C_8	DQ3_8C_8				
8C	VREFB8CN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	P28									
8B	VREFB8BN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	L28	DQ7T	DQ4T	DQ2T	DQ2_8B_0	DQ2_8B_0				
8B	VREFB8BN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	M28	DQ7T	DQ4T	DQ2T	DQ2_8B_1	DQ2_8B_1				
8B	VREFB8BN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	H28	DQ7T	DQ4T	DQ2T	DQ2_8B_2	DQ2_8B_2				
8B	VREFB8BN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	J28									
8B	VREFB8BN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	C28	DQ7T	DQ4T	DQ2T	DQ2_8B_3	DQ2_8B_3				

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
8B	VREFB8BN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	D28	DQ7T	DQ4T	DQ2T	DQ2_8B_4	DQ2_8B_4				
8B	VREFB8BN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	F28	DQ7T	DQ4T	DQ2T	DQ2_8B_5	DQ2_8B_5				
8B	VREFB8BN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	G28									
8B	VREFB8BN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	R29	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS2_8B	DQS2_8B				
8B	VREFB8BN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	T29	DQSn7T/QK7T	DQSn4T/QK4T	DQ2T	DQS#2_8B	DQS#2_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	J29	DQ7T	DQ4T	DQ2T	DM2_8B	DM2_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	K29									
8B	VREFB8BN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	M29	DQ7T	DQ4T	DQ2T	DQ2_8B_6	DQ2_8B_6				
8B	VREFB8BN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	N29	DQ7T	DQ4T	DQ2T	DQ2_8B_7	DQ2_8B_7				
8B	VREFB8BN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	F29	DQ7T	DQ4T	DQ2T	DQ2_8B_8	DQ2_8B_8				
8B	VREFB8BN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	G29									
8B	VREFB8BN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	B28	DQ8T	DQ4T	DQ2T	DQ1_8B_0	DQ1_8B_0				
8B	VREFB8BN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	C29	DQ8T	DQ4T	DQ2T	DQ1_8B_1	DQ1_8B_1				
8B	VREFB8BN0	IO					R30	DQ8T	DQ4T	DQ2T	DQ1_8B_2	DQ1_8B_2				
8B	VREFB8BN0	IO	VREFB8BN0				R31									
8B	VREFB8BN0	IO			DIFFIO_RX_T86p	DIFFOUT_T86p	A29	DQ8T	DQ4T	DQ2T	DQ1_8B_3	DQ1_8B_3				
8B	VREFB8BN0	IO			DIFFIO_RX_T86n	DIFFOUT_T86n	A28	DQ8T	DQ4T	DQ2T	DQ1_8B_4	DQ1_8B_4				
8B	VREFB8BN0	IO			DIFFIO_TX_T87p	DIFFOUT_T87p	L30	DQ8T	DQ4T	DQ2T	DQ1_8B_5	DQ1_8B_5				
8B	VREFB8BN0	IO			DIFFIO_TX_T87n	DIFFOUT_T87n	M30									
8B	VREFB8BN0	IO			DIFFIO_RX_T88p	DIFFOUT_T88p	N30	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	DQ2T	DQS1_8B	DQS1_8B				
8B	VREFB8BN0	IO			DIFFIO_RX_T88n	DIFFOUT_T88n	P30	DQSn8T/QK8T	DQ4T	DQ2T	DQS#1_8B	DQS#1_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T89p	DIFFOUT_T89p	J30	DQ8T	DQ4T	DQ2T	DM1_8B	DM1_8B				
8B	VREFB8BN0	IO			DIFFIO_TX_T89n	DIFFOUT_T89n	K30									
8B	VREFB8BN0	IO			DIFFIO_RX_T90p	DIFFOUT_T90p	D30	DQ8T	DQ4T	DQ2T	DQ1_8B_6	DQ1_8B_6				
8B	VREFB8BN0	IO			DIFFIO_RX_T90n	DIFFOUT_T90n	D29	DQ8T	DQ4T	DQ2T	DQ1_8B_7	DQ1_8B_7				
8B	VREFB8BN0	IO			DIFFIO_TX_T91p	DIFFOUT_T91p	F30	DQ8T	DQ4T	DQ2T	DQ1_8B_8	DQ1_8B_8				
8B	VREFB8BN0	IO			DIFFIO_TX_T91n	DIFFOUT_T91n	G30				RESET#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T92p	DIFFOUT_T92p	B30	DQ9T	DQ5T		CK_8A	CK_8A				
8A	VREFB8AN0	IO			DIFFIO_RX_T92n	DIFFOUT_T92n	C30	DQ9T	DQ5T		CK#_8A	CK#_8A				
8A	VREFB8AN0	IO			DIFFIO_TX_T93p	DIFFOUT_T93p	E31	DQ9T	DQ5T		CKE_8A_0	CKE_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T93n	DIFFOUT_T93n	F31				CKE_8A_1	CKE_8A_1				
8A	VREFB8AN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	B31	DQ9T	DQ5T		A_8A_0	CA_8A_0				
8A	VREFB8AN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	A30	DQ9T	DQ5T		A_8A_1	CA_8A_1				
8A	VREFB8AN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	A31	DQ9T	DQ5T		A_8A_2	CA_8A_2				
8A	VREFB8AN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	A32				A_8A_3	CA_8A_3				
8A	VREFB8AN0	IO			DIFFIO_RX_T96p	DIFFOUT_T96p	A33	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		A_8A_4	CA_8A_4				
8A	VREFB8AN0	IO			DIFFIO_RX_T96n	DIFFOUT_T96n	B33	DQSn9T/QK9T	DQSn5T/QK5T		A_8A_5	CA_8A_5				
8A	VREFB8AN0	IO			DIFFIO_TX_T97p	DIFFOUT_T97p	H31	DQ9T	DQ5T		A_8A_6	CA_8A_6				
8A	VREFB8AN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	J31				A_8A_7	CA_8A_7				
8A	VREFB8AN0	IO			DIFFIO_RX_T98p	DIFFOUT_T98p	C31	DQ9T	DQ5T		A_8A_8	CA_8A_8				
8A	VREFB8AN0	IO			DIFFIO_RX_T98n	DIFFOUT_T98n	D31	DQ9T	DQ5T		A_8A_9	CA_8A_9				
8A	VREFB8AN0	IO			DIFFIO_TX_T99p	DIFFOUT_T99p	C32	DQ9T	DQ5T		A_8A_10					
8A	VREFB8AN0	IO			DIFFIO_TX_T99n	DIFFOUT_T99n	D32				A_8A_11					
8A	VREFB8AN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	N31	DQ10T	DQ5T		A_8A_12					
8A	VREFB8AN0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	P31	DQ10T	DQ5T		A_8A_13					
8A	VREFB8AN0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	J32	DQ10T	DQ5T		A_8A_14					
8A	VREFB8AN0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	K32				A_8A_15					
8A	VREFB8AN0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	M32	DQ10T	DQ5T		BA_8A_0					
8A	VREFB8AN0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	N32	DQ10T	DQ5T		BA_8A_1					
8A	VREFB8AN0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	J34	DQ10T	DQ5T		BA_8A_2					
8A	VREFB8AN0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	K34				RAS#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	L33	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		CAS#_8A					
8A	VREFB8AN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	M33	DQSn10T/QK10T	DQ5T		WE#_8A					
8A	VREFB8AN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	L31	DQ10T	DQ5T		ODT_8A_0	ODT_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	M31				ODT_8A_1	ODT_8A_1				
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T106p	DIFFOUT_T106p	N34	DQ10T	DQ5T							
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T106n	DIFFOUT_T106n	N33	DQ10T	DQ5T							
8A	VREFB8AN0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	L34	DQ10T	DQ5T		CS#_8A_0	CS#_8A_0				
8A	VREFB8AN0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	M34				CS#_8A_1	CS#_8A_1				
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T108p	DIFFOUT_T108p	E34	DQ11T								
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T108n	DIFFOUT_T108n	F34	DQ11T								
8A	VREFB8AN0	IO					J33	DQ11T								
8A	VREFB8AN0	IO	VREFB8AN0				H33									
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T109p	DIFFOUT_T109p	B34	DQ11T								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T109n	DIFFOUT_T109n	A35	DQ11T								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T110p	DIFFOUT_T110p	C33	DQ11T								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T110n	DIFFOUT_T110n	D33									
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T111p	DIFFOUT_T111p	G34	DQS11T/CQ11T/CQn11T/QKn11T								
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T111n	DIFFOUT_T111n	H34	DQSn11T/QK11T								
8A	VREFB8AN0	IO			DIFFIO_TX_T112p	DIFFOUT_T112p	F32	DQ11T								
8A	VREFB8AN0	IO			DIFFIO_TX_T112n	DIFFOUT_T112n	G32									
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T113p	DIFFOUT_T113p	C34	DQ11T								
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T113n	DIFFOUT_T113n	D34	DQ11T								
8A	VREFB8AN0	IO			DIFFIO_TX_T114p	DIFFOUT_T114p	E33	DQ11T								
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T114n	DIFFOUT_T114n	F33									
8A		MSEL0		MSEL0			H35									
8A		MSEL1		MSEL1			A34									
8A		MSEL2		MSEL2			D35									
8A		MSEL3		MSEL3			A37									
8A		MSEL4		MSEL4			P34									
8A		CONF_DONE		CONF_DONE			K35									
8A		nSTATUS		nSTATUS			F35									
8A		nCE		nCE			M35									
8A		nCONFIG		nCONFIG			A36									
		GND					P35									
		VCC_HPS					V16									
		GND					W16									
		GND					AA33									
		GND					AA35									
		GND					AA38									
		GND					AA39									
		GND					AB31									
		GND					AB32									
		GND					AB34									
		GND					AB36									
		GND					AB37									
		GND					AC33									
		GND					AC38									
		GND					AC39									
		GND					AD32									
		GND					AD36									
		GND					AD37									
		GND					AE33									
		GND					AE35									
		GND					AE38									
		GND					AE39									
		GND					AF31									
		GND					AF32									
		GND					AF34									
		GND					AF36									
		GND					AF37									
		GND					AG38									
		GND					AG39									
		GND					AH32									
		GND					AH33									
		GND					AH34									
		GND					AH35									
		GND					AH36									
		GND					AH37									
		GND					AJ35									

Bank Number	VREF	PinName/Function *(2)*, *(3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AJ38									
		GND					AJ39									
		GND					AK36									
		GND					AK37									
		GND					AL35									
		GND					AL38									
		GND					AL39									
		GND					AM36									
		GND					AM37									
		GND					AN35									
		GND					AN38									
		GND					AN39									
		GND					AP36									
		GND					AP37									
		GND					AR35									
		GND					AR38									
		GND					AR39									
		GND					AT36									
		GND					AT37									
		GND					AU35									
		GND					AU38									
		GND					AU39									
		GND					AV35									
		GND					AV36									
		GND					AV37									
		GND					AV38									
		GND					AV39									
		GND					AW35									
		GND					AW38									
		GND					B36									
		GND					B37									
		GND					C35									
		GND					C38									
		GND					C39									
		GND					D36									
		GND					D37									
		GND					E35									
		GND					E38									
		GND					E39									
		GND					F36									
		GND					F37									
		GND					G35									
		GND					G38									
		GND					G39									
		GND					H36									
		GND					H37									
		GND					J35									
		GND					J38									
		GND					J39									
		GND					K36									
		GND					K37									
		GND					L35									
		GND					L38									
		GND					L39									
		GND					M36									
		GND					M37									
		GND					N35									
		GND					N38									
		GND					N39									
		GND					P36									
		GND					P37									
		GND					R34									
		GND					R38									
		GND					R39									
		GND					T32									
		GND					T36									
		GND					T37									
		GND					U33									
		GND					U35									
		GND					U38									
		GND					U39									
		GND					V32									
		GND					V34									
		GND					V36									
		GND					V37									
		GND					W33									
		GND					W38									
		GND					W39									
		GND					Y31									
		GND					Y32									
		GND					Y36									
		GND					Y37									
		GND					AA3									
		GND					AA4									
		GND					AA6									
		GND					AA8									
		GND					AB1									
		GND					AB2									
		GND					AB7									
		GND					AC3									
		GND					AC4									
		GND					AC8									
		GND					AD1									
		GND					AD2									
		GND					AD5									
		GND					AD7									
		GND					AE3									
		GND					AE4									
		GND					AE6									
		GND					AE8									
		GND					AF1									
		GND					AF2									
		GND					AF9									
		GND					AG3									
		GND					AG4									
		GND					AG5									
		GND					AG6									
		GND					AG7									
		GND					AG8									
		GND					AH1									
		GND					AH2									
		GND					AH5									
		GND					AJ3									
		GND					AJ4									
		GND					AK1									
		GND					AK2									
		GND					AK5									
		GND					AL3									
		GND					AL4									
		GND					AM1									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AM2									
		GND					AM5									
		GND					AN3									
		GND					AN4									
		GND					AP1									
		GND					AP2									
		GND					AP5									
		GND					AR3									
		GND					AR4									
		GND					AT1									
		GND					AT2									
		GND					AT5									
		GND					AU3									
		GND					AU4									
		GND					AV1									
		GND					AV2									
		GND					N3									
		GND					N4									
		GND					P1									
		GND					P2									
		GND					P5									
		GND					R3									
		GND					R4									
		GND					R5									
		GND					T1									
		GND					T2									
		GND					T5									
		GND					U3									
		GND					U4									
		GND					U5									
		GND					U6									
		GND					V1									
		GND					V2									
		GND					V7									
		GND					W3									
		GND					W4									
		GND					W8									
		GND					Y1									
		GND					Y2									
		GND					Y5									
		GND					Y7									
		VCCP					AA21									
		VCCP					AA25									
		VCCP					AB15									
		VCCP					U10									
		VCCP					U16									
		VCCP					V25									
		VCCP					V27									
		VCCP					W10									
		VCCP					Y27									
		VCCA_FPLL					AC30									
		VCCA_FPLL					AC9									
		VCCA_FPLL					Y30									
		VCCA_FPLL					AA9									
		VCCA_FPLL					V31									
		VCCPLL_HPS					U8									
		VCCBAT					R33									
		VCC_AUX					AB14									
		VCC_AUX					AB26									
		VCC_AUX					U28									
		VCC_AUX_SHARED					U15									
		VCCD_FPLL					AD31									
		VCCD_FPLL					AE9									
		VCCD_FPLL					W30									
		VCCD_FPLL					W9									
		VCCD_FPLL					T31									
		VCCA_GXBL0					AF33									
		VCCA_GXBR0					AE7									
		VCCA_GXBL1					AB33									
		VCCA_GXBR1					AA7									
		VCCA_GXBL2					Y33									
		VCCH_GXBL0					AD33									
		VCCH_GXBR0					AC7									
		VCCH_GXBL1					Y33									
		VCCH_GXBR1					W7									
		VCCH_GXBL2					T33									
		VCCL_GXBL0					AD34									
		VCCL_GXBL0					AD35									
		VCCL_GXBR0					AC5									
		VCCL_GXBR0					AC6									
		VCCL_GXBL1					Y34									
		VCCL_GXBL1					Y35									
		VCCL_GXBR1					W5									
		VCCL_GXBR1					W6									
		VCCL_GXBL2					T34									
		VCCL_GXBL2					T35									
		VCCR_GXBL					U34									
		VCCR_GXBL					W34									
		VCCR_GXBL					AA34									
		VCCR_GXBL					AB35									
		VCCR_GXBL					AC35									
		VCCR_GXBL					AE34									
		VCCR_GXBL					AF35									
		VCCR_GXBR					V5									
		VCCR_GXBR					V6									
		VCCR_GXBR					Y6									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AB5									
		VCCR_GXBR					AB6									
		VCCT_GXBL0					AG35									
		VCCT_GXBL0					AG34									
		VCCT_GXBR0					AD6									
		VCCT_GXBR0					AE5									
		VCCT_GXBL1					W35									
		VCCT_GXBL1					V35									
		VCCT_GXBR1					AF5									
		VCCT_GXBR1					AF6									
		VCCT_GXBL2					R35									
		VCCT_GXBL2					AC34									
		VCC					AA10									
		VCC					AA12									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA20									
		VCC					AA22									
		VCC					AA24									
		VCC					AA26									
		VCC					AB11									
		VCC					AB17									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					U18									
		VCC					V17									
		VCC					V22									
		VCC					V23									
		VCC					V29									
		VCC					W20									
		VCC					W18									
		VCC					W22									
		VCC					W24									
		VCC					W26									
		VCC					W28									
		VCC					Y11									
		VCC					Y15									
		VCC					Y17									
		VCC					Y19									
		VCC					Y23									
		VCC					Y25									
		VCC					Y29									
		VCC					Y21									
		VCC_HPS					U12									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					V15									
		VCC_HPS					W12									
		VCC_HPS					W14									
		VCC_HPS					Y13									
		VCCIO3A					AH29									
		VCCIO3A					AJ30									
		VCCIO3A					AK35									
		VCCIO3A					AM30									
		VCCIO3A					AP35									
		VCCIO3A					AT35									
		VCCIO3B					AK28									
		VCCIO3B					AL27									
		VCCIO3B					AN28									
		VCCIO3B					AT28									
		VCCIO3C					AJ24									
		VCCIO3C					AL25									
		VCCIO3C					AM24									
		VCCIO3C					AP25									
		VCCIO3C					AR24									
		VCCIO3C					AU25									
		VCCIO3D					AJ22									
		VCCIO3D					AL21									
		VCCIO3D					AM22									
		VCCIO3D					AP21									
		VCCIO3D					AR22									
		VCCIO3D					AU21									
		VCCIO4A					AG10									
		VCCIO4A					AJ5									
		VCCIO4A					AL5									
		VCCIO4A					AM5									
		VCCIO4A					AR5									
		VCCIO4A					AU5									
		VCCIO4B					AK13									
		VCCIO4B					AM12									
		VCCIO4B					AN10									
		VCCIO4B					AN13									
		VCCIO4B					AR12									
		VCCIO4B					AT10									
		VCCIO4C					AJ15									
		VCCIO4C					AM15									
		VCCIO4C					AR15									
		VCCIO4C					AV15									
		VCCIO4D					AJ19									
		VCCIO4D					AK18									
		VCCIO4D					AM19									
		VCCIO4D					AN18									
		VCCIO4D					AR19									
		VCCIO4D					AT18									
		VCCIO6A_HPS					A10									
		VCCIO6A_HPS					C5									
		VCCIO6A_HPS					C8									
		VCCIO6A_HPS					F6									
		VCCIO6A_HPS					F8									
		VCCIO6A_HPS					J6									
		VCCIO6A_HPS					K8									
		VCCIO6A_HPS					M8									
		VCCIO6A_HPS					P9									
		VCCIO6B_HPS					B3									
		VCCIO6B_HPS					D4									
		VCCIO6B_HPS					G3									
		VCCIO6B_HPS					J3									
		VCCIO6B_HPS					L3									
		VCCIO6B_HPS					N2									
		VCCIO6B_HPS					N5									
		VCCIO7A_HPS					B13									
		VCCIO7A_HPS					E10									
		VCCIO7A_HPS					G12									
		VCCIO7A_HPS					K13									
		VCCIO7B_HPS					E14									
		VCCIO7B_HPS					J15									
		VCCIO7C_HPS					D17									
		VCCIO7D_HPS					B18									
		VCCIO7D_HPS					G17									
		VCCIO7E_HPS					J20									
		VCCIO7G					K19									
		VCCIO8A					B35									
		VCCIO8A					G31									
		VCCIO8A					G33									
		VCCIO8A					K31									
		VCCIO8A					K33									
		VCCIO8A					P33									
		VCCIO8B					E28									
		VCCIO8B					E30									
		VCCIO8B					H30									
		VCCIO8B					K28									
		VCCIO8C					C25									
		VCCIO8C					D27									
		VCCIO8C					F26									
		VCCIO8C					G27									
		VCCIO8C					J25									
		VCCIO8C					M24									
		VCCIO8D					C21									
		VCCIO8D					D22									
		VCCIO8D					F21									
		VCCIO8D					G22									
		VCCIO8D					K22									
		VCCIO8D					M21									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD3					AA27									
		VCCPD3					AA28									
		VCCPD3					AA29									
		VCCPD3					AB22									
		VCCPD3					AB23									
		VCCPD3					AB24									
		VCCPD3					AB30									
		VCCPD4A					AC10									
		VCCPD4A					AE10									
		VCCPD4BCD					AB12									
		VCCPD4BCD					AB13									
		VCCPD4BCD					AB16									
		VCCPD4BCD					AB18									
		VCCPD4BCD					AB19									
		VCCPD6A6B_HPS					L9									
		VCCPD6A6B_HPS					T10									
		VCCPD6A6B_HPS					T6									
		VCCPD6A6B_HPS					T8									
		VCCPD7A_HPS					R12									
		VCCPD7B_HPS					T14									
		VCCPD7C_HPS					R16									
		VCCPD7D_HPS					T17									
		VCCPD7E_HPS					R18									
		VCCPD7FG					U21									
		VCCPD8					R32									
		VCCPD8					T30									
		VCCPD8					U22									
		VCCPD8					U24									
		VCCPD8					U26									
		VCCPD8					U29									
		VCCPGM					J19									
		VCCPGM					AG29									
		VCCRSTCLK_HPS					L10									
		VCC_HPS					T13									
		VCC_HPS					U14									
		VCC_HPS					U9									
		VCC_HPS					V10									
	VREFB7A7B7C7D7EN0_HPS	VREFB7A7B7C7D7EN0_HPS					P18									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA19									
		GND					AA23									
		GND					AA30									
		GND					AB10									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AC26									
		GND					AC28									
		GND					AD10									
		GND					AD30									
		GND					AE30									
		GND					AF11									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF26									
		GND					AF29									
		GND					AF30									
		GND					AG31									
		GND					AG9									
		GND					AJ11									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									
		GND					AJ23									
		GND					AJ26									
		GND					AJ29									
		GND					AJ32									
		GND					AJ8									
		GND					AM11									
		GND					AM14									
		GND					AM17									
		GND					AM20									
		GND					AM23									
		GND					AM26									
		GND					AM29									
		GND					AM32									
		GND					AM8									
		GND					AR11									
		GND					AR14									
		GND					AR17									
		GND					AR20									
		GND					AR23									
		GND					AR26									
		GND					AR29									
		GND					AR32									
		GND					AR8									
		GND					AV11									
		GND					AV14									
		GND					AV17									
		GND					AV20									
		GND					AV23									
		GND					AV26									
		GND					AV29									
		GND					AV32									
		GND					AV5									
		GND					AV8									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B20									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B32									
		GND					B5									
		GND					B8									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									

Bank Number	VREF	PinName/Function *(2), (3)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 *(4)*	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 *(5)*	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					E32									
		GND					E5									
		GND					E8									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					J14									
		GND					K20									
		GND					L11									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L5									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P8									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T9									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U25									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V9									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					Y10									
		GND					Y12									
		GND					Y14									
		GND					Y16									
		GND					Y18									
		GND					Y20									
		GND					Y22									
		GND					Y24									
		GND					Y26									
		GND					Y28									

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) Pins with * contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.
(4) Pins with * are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the Transceiver Clocking in Arria V Devices chapter.
(5) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	'-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.