Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		DNU					C25			
		DNU					D25			
		RREF_TL					D26			
GXB_L1		GXB_TX_L8n					E23			
GXB_L1		GXB_TX_L8p					E24			
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					F26			
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					F25			
GXB_L1		GXB_TX_L7n					G23			
GXB_L1		GXB_TX_L7p					G24			
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					H26			
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					H25			
GXB_L1		GXB_TX_L6n					J23			
GXB_L1		GXB_TX_L6p					J24			
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					K26			
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					K25			
GXB_L1		REFCLK2Ln					N19			
GXB_L1		REFCLK2Lp					N18			
GXB_L0		REFCLK1Ln					R19			
GXB_L0		REFCLK1Lp					R18			
GXB_L0		GXB_TX_L5n					L23			
GXB_L0		GXB_TX_L5p					L24			
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					M26			
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					M25			
GXB_L0		GXB_TX_L4n					N23			
GXB_L0		GXB_TX_L4p					N24			
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					P26			
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					P25			
GXB_L0		GXB_TX_L3n					R23			
GXB_L0		GXB_TX_L3p					R24			
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					T26			
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					T25			
GXB_L0		GXB_TX_L2n					U23			
GXB_L0		GXB_TX_L2p					U24			
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					V26			
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					V25			
GXB_L0		GXB_TX_L1n					W23			
GXB_L0		GXB_TX_L1p					W24			
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					Y26			
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					Y25			
GXB_L0		GXB_TX_L0n					AA23			
GXB_L0		GXB_TX_L0p					AA24			
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AB26			
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AB25			
GXB_L0		REFCLK0Ln					U19			
GXB_L0		REFCLK0Lp					U18			
		DNU					Y22			
3A		TDO		TDO			AE26			
3A		TMS		TMS			AB22			
3A		TCK		TCK			AD24			
3A		TDI		TDI			AC23			
3A		DCLK		DCLK			AE24			
3A		nCSO		DATA4			AD26			
3A		AS_DATA3		DATA3			AD25			
3A		AS_DATA2		DATA2			AF25			
3A		AS_DATA1		DATA1			AE25			
3A		AS_DATA0,ASDO		DATA0			AF24			
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AB21			
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AC21	DQ1B		
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AC22	DQ1B		
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AD22	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	Y21			
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AA21	DQ1B		
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	W20	DQSn1B/QK1B		
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	W21	DQS1B/CQ1B/CQn1B/QKn1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AD23			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AE23	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AE21	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AF22	DQ1B		
3A	VREFB3AN0	IO	VREFB3AN0				Y20			
3A	VREFB3AN0	IO					Y19	DQ1B		
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AC20	DQ1B		
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AD20	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AF21			
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AF20			
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AE19			
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AF19			
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AA19			
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AB19			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AC19			
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AD19			
3D	VREFB3DN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AA18			
3D	VREFB3DN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AB18			
3D	VREFB3DN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	W18			
3D	VREFB3DN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	Y18			
3D	VREFB3DN0	IO	VREFB3DN0				Y17			
3D	VREFB3DN0	IO					AA17			
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B60n	DIFFOUT_B60n	AD18			
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B60p	DIFFOUT_B60p	AE18			
3D	VREFB3DN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AA16			
3D	VREFB3DN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AB16			
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B62n	DIFFOUT_B62n	AC17			
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B62p	DIFFOUT_B62p	AD17			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B63n	DIFFOUT_B63n	U16			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B63p	DIFFOUT_B63p	V16			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B64n	DIFFOUT_B64n	W16			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B64p	DIFFOUT_B64p	Y16			
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B66n	DIFFOUT_B66n	AF17			
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B66p	DIFFOUT_B66p	AF18			
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B68n	DIFFOUT_B68n	AD16			
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B68p	DIFFOUT_B68p	AE16			
		VCCD_FPLL					U13			
		VCCA_FPLL					U12			
		DNU					T14			
4D	VREFB4DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	Y14			
4D	VREFB4DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AA14	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AA15	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AB15	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	V15			
4D	VREFB4DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	W15	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	U14	DQSn2B/QK2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	V14	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	W13			
4D	VREFB4DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	Y13	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AC15	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AD15	DQ2B	DQ1B	
4D	VREFB4DN0	IO	VREFB4DN0				AB13			
4D	VREFB4DN0	IO					AA13	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AC14	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AD14	DQ2B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AE15			
4D	VREFB4DN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AF15	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AC13	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AD13	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	V11			
4D	VREFB4DN0	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	V12	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AB12	DQSn3B/QK3B	DQSn1B/QK1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AC12	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	W12			
4D	VREFB4DN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	Y12	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AF14	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81p	DIFFOUT_B81p	AE13	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_TX_B82n	DIFFOUT_B82n	Y11			
4D	VREFB4DN0	IO			DIFFIO_TX_B82p	DIFFOUT_B82p	AA11	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AC11	DQ3B	DQ1B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AD11	DQ3B	DQ1B	
4C	VREFB4CN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AE12			
4C	VREFB4CN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AF12	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B85n	DIFFOUT_B85n	U10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B85p	DIFFOUT_B85p	V10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B86n	DIFFOUT_B86n	Y9			
4C	VREFB4CN0	IO			DIFFIO_TX_B86p	DIFFOUT_B86p	AA9	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	W9	DQSn4B/QK4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	W10	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AF11			
4C	VREFB4CN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AF10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AA10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AB10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO	VREFB4CN0				AB9			
4C	VREFB4CN0	IO					AC9	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AD10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AE10	DQ4B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AD9			
4C	VREFB4CN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AE9	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AF8	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AF9	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	Y7			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4C	VREFB4CN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AA7	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	Y8	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AA8	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AB7			
4C	VREFB4CN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AC7	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AC8	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AD8	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	V8			
4C	VREFB4CN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	W7	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AE7	DQ5B	DQ2B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AD6	DQ5B	DQ2B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AE6			
4B	VREFB4BN0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AF6	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B100n	DIFFOUT_B100n	AF4	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B100p	DIFFOUT_B100p	AF5	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B101n	DIFFOUT_B101n	AB6			
4B	VREFB4BN0	IO			DIFFIO_TX_B101p	DIFFOUT_B101p	AC6	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B102n	DIFFOUT_B102n	AD5	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B
4B	VREFB4BN0	IO			DIFFIO_RX_B102p	DIFFOUT_B102p	AE4	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B
4B	VREFB4BN0	IO			DIFFIO_TX_B103n	DIFFOUT_B103n	AF3			
4B	VREFB4BN0	IO			DIFFIO_TX_B103p	DIFFOUT_B103p	AF2	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B104n	DIFFOUT_B104n	AD3	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B104p	DIFFOUT_B104p	AE3	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B105n	DIFFOUT_B105n	AC5			
4B	VREFB4BN0	IO			DIFFIO_TX_B105p	DIFFOUT_B105p	AC4	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B106n	DIFFOUT_B106n	AE1	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B106p	DIFFOUT_B106p	AD2	DQ6B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AC3			
4B	VREFB4BN0	IO			DIFFIO_TX_B107p	DIFFOUT_B107p	AC2	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B108n	DIFFOUT_B108n	AB1	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B108p	DIFFOUT_B108p	AC1	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B109n	DIFFOUT_B109n	Y5			
4B	VREFB4BN0	IO			DIFFIO_TX_B109p	DIFFOUT_B109p	AA5	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B110n	DIFFOUT_B110n	AB4	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B110p	DIFFOUT_B110p	AB3	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B111n	DIFFOUT_B111n	AA2			
4B	VREFB4BN0	IO			DIFFIO_TX_B111p	DIFFOUT_B111p	AA1	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B112n	DIFFOUT_B112n	Y3	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B112p	DIFFOUT_B112p	Y2	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO	VREFB4BN0				Y6			
4B	VREFB4BN0	IO					W6	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AA4	DQ7B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AA3	DQ7B	DQ3B	DQ1B
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B114n	DIFFOUT_B114n	W1			
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B114p	DIFFOUT_B114p	V1	DQ8B		
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B115n	DIFFOUT_B115n	V3	DQ8B		
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B115p	DIFFOUT_B115p	W3	DQ8B		
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B116n	DIFFOUT_B116n	V4			
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B116p	DIFFOUT_B116p	W4	DQ8B		
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B117n	DIFFOUT_B117n	V2	DQSn8B/QK8B		
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B117p	DIFFOUT_B117p	U2	DQS8B/CQ8B/CQn8B/QKn8B		
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B118n	DIFFOUT_B118n	U1			
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B118p	DIFFOUT_B118p	T1	DQ8B		
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B119n	DIFFOUT_B119n	T3	DQ8B		
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B119p	DIFFOUT_B119p	U3	DQ8B		
4A	VREFB4AN0	IO	VREFB4AN0				V5			
4A	VREFB4AN0	IO					U5	DQ8B		
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B120n	DIFFOUT_B120n	R3	DQ8B		
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B120p	DIFFOUT_B120p	P3	DQ8B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B121n	DIFFOUT_B121n	R4			
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B121p	DIFFOUT_B121p	T4			
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B122n	DIFFOUT_B122n	N4			
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B122p	DIFFOUT_B122p	N3			
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B124n	DIFFOUT_B124n	N6			
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B124p	DIFFOUT_B124p	P7			
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B126n	DIFFOUT_B126n	R5			
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B126p	DIFFOUT_B126p	P5			
4A	VREFB4AN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	T6			
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B127p	DIFFOUT_B127p	U6			
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B128n	DIFFOUT_B128n	P6			
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B128p	DIFFOUT_B128p	R6			
		RREF_BR					P1			
		DNU					P2			
		DNU					R2			
		DNU					M4			
		GND					M3			
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	L6			
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	M6			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	J5			
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	K5			
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	K4			
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	L4			
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	M1			
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	M2			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	K1			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	L1			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J3			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K3			
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	J2	DQ1T		
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	K2	DQ1T		
7A	VREFB7AN0	IO					H3	DQ1T		
7A	VREFB7AN0	IO	VREFB7AN0				H4			
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	G1	DQ1T		
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	H1	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFOUT_T11p	F3	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T11n	DIFFOUT_T11n	G3			
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	F2	DQS1T/CQ1T/CQn1T/QKn1T		
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	G2	DQSn1T/QK1T		
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	G5	DQ1T		
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	G4			
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	E1	DQ1T		
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	F1	DQ1T		
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	E3	DQ1T		
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	E4			
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	D2	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	D3	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO					F5	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO	VREFB7BN0				F6			
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C1	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	D1	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C2	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C3			
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	D4	DQS2T/CQ2T/CQn2T/QKn2T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	D5	DQSn2T/QK2T	DQSn1T/QK1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	H6	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	J6			
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	A2	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	B1	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B3	DQ2T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	B4			
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	J7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	K7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	G7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	H7			
7B	VREFB7BN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	D6	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	D7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C5	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C6			
7B	VREFB7BN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	A4	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS1T/CQ1T/CQn1T/QKn1T
7B	VREFB7BN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	A5	DQSn3T/QK3T	DQ1T	DQSn1T/QK1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	E7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F7			
7B	VREFB7BN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	B6	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	B7	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	A6	DQ3T	DQ1T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A7			
7C	VREFB7CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	D9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	E9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	K9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	J8			
7C	VREFB7CN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	F8	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	G8	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C8	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	D8			
7C	VREFB7CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	F9	DQS4T/CQ4T/CQn4T/QKn4T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	G9	DQSn4T/QK4T	DQSn2T/QK2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	H9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	J9			
7C	VREFB7CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	A8	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	B9	DQ4T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	C10			
7C	VREFB7CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	H10	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	J10	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO					E10	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO	VREFB7CN0				F10			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7C	VREFB7CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	A11	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	B10	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	C11	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	D11			
7C	VREFB7CN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	J11	DQS5T/CQ5T/CQn5T/QKn5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	K11	DQSn5T/QK5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	F11	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	G11			
7C	VREFB7CN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	A12	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	B12	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	C12	DQ5T	DQ2T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	D12			
7D	VREFB7DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	B13	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	C13	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	F12	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	G12			
7D	VREFB7DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	H12	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	J12	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	A14	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	B15			
7D	VREFB7DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	E12	DQS6T/CQ6T/CQn6T/QKn6T	DQS3T/CQ3T/CQn3T/QKn3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	E13	DQSn6T/QK6T	DQSn3T/QK3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	H13	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	J13			
7D	VREFB7DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	F13	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	G13	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	C14	DQ6T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	D14			
7D	VREFB7DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	A16	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	B16	DQ7T	DQ3T	
7D	VREFB7DN0	IO					G14	DQ7T	DQ3T	
7D	VREFB7DN0	IO	VREFB7DN0				F14			
7D	VREFB7DN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	G15	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	H15	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	C15	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	C16			
7D	VREFB7DN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	J15	DQS7T/CQ7T/CQn7T/QKn7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	K15	DQSn7T/QK7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	E15	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	F15			
7D	VREFB7DN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	J14	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	K14	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	D16	DQ7T	DQ3T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	E16			
		VCCA_FPLL					L12			
		VCCD_FPLL					L13			
		DNU					K12			
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	H16			
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	J16			
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	J17			
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	K17			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	C17			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	D17			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	F16			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	G16			
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T67p	DIFFOUT_T67p	B18			
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T67n	DIFFOUT_T67n	A17			
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	A19			
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	B19			
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T69p	DIFFOUT_T69p	C18			
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T69n	DIFFOUT_T69n	D18			
8D	VREFB8DN0	IO					F17			
8D	VREFB8DN0	IO	VREFB8DN0				G17			
8D	VREFB8DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	J18			
8D	VREFB8DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	K18			
8D	VREFB8DN0	IO			DIFFIO_TX_T71p	DIFFOUT_T71p	F18			
8D	VREFB8DN0	IO			DIFFIO_TX_T71n	DIFFOUT_T71n	G18			
8A	VREFB8AN0	IO			DIFFIO_RX_T118p	DIFFOUT_T118p	D19			
8A	VREFB8AN0	IO			DIFFIO_RX_T118n	DIFFOUT_T118n	E19			
8A	VREFB8AN0	IO			DIFFIO_TX_T119p	DIFFOUT_T119p	F19			
8A	VREFB8AN0	IO			DIFFIO_TX_T119n	DIFFOUT_T119n	G19			
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T120p	DIFFOUT_T120p	C20			
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T120n	DIFFOUT_T120n	C19			
8A	VREFB8AN0	IO			DIFFIO_TX_T121p	DIFFOUT_T121p	B21			
8A	VREFB8AN0	IO			DIFFIO_TX_T121n	DIFFOUT_T121n	C21			
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T122p	DIFFOUT_T122p	A20	DQ8T		
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T122n	DIFFOUT_T122n	A21	DQ8T		
8A	VREFB8AN0	IO					F20	DQ8T		

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8A	VREFB8AN0	IO	VREFB8AN0				G20			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T123p	DIFFOUT_T123p	A23	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T123n	DIFFOUT_T123n	A22	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T124p	DIFFOUT_T124p	D20	DQ8T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T124n	DIFFOUT_T124n	D21			
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T125p	DIFFOUT_T125p	H19	DQS8T/CQ8T/CQn8T/QKn8T		
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T125n	DIFFOUT_T125n	J20	DQSn8T/QK8T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	G21	DQ8T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	H21			
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T127p	DIFFOUT_T127p	B22	DQ8T		
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T127n	DIFFOUT_T127n	C22	DQ8T		
8A	VREFB8AN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	E21	DQ8T		
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T128n	DIFFOUT_T128n	F21			
8A		MSEL0		MSEL0			A25			
8A		MSEL1		MSEL1			C24			
8A		MSEL2		MSEL2			B25			
8A		MSEL3		MSEL3			B26			
8A		MSEL4		MSEL4			J21			
8A		CONF_DONE		CONF_DONE			C23			
8A		nSTATUS		nSTATUS			B24			
8A		nCE		nCE			A24			
8A		nCONFIG		nCONFIG			L18			
		GND					K19			
		GND					AA22			
		GND					AA25			
		GND					AA26			
		GND					AB23			
		GND					AB24			
		GND					AC24			
		GND					AC25			
		GND					AC26			
		GND					C26			
		GND					D23			
		GND					D24			
		GND					E22			
		GND					E25			
		GND					E26			
		GND					F23			
		GND					F24			
		GND					G22			
		GND					G25			
		GND					G26			
		GND					H23			
		GND					H24			
		GND					J22			
		GND					J25			
		GND					J26			
		GND					K21			
		GND					K23			
		GND					K24			
		GND					L22			
		GND					L25			
		GND					L26			
		GND					M19			
		GND					M23			
		GND					M24			
		GND					N20			
		GND					N22			
		GND					N25			
		GND					N26			
		GND					P19			
		GND					P23			
		GND					P24			
		GND					R20			
		GND					R22			
		GND					R25			
		GND					R26			
		GND					T19			
		GND					T21			
		GND					T23			
		GND					T24			
		GND					U20			
		GND					U25			
		GND					U26			
		GND					V18			
		GND					V19			
		GND					V22			
		GND					V23			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					V24			
		GND					W22			
		GND					W25			
		GND					W26			
		GND					Y23			
		GND					Y24			
		VCCP					L11			
		VCCP					L15			
		VCCP					L9			
		VCCP					M8			
		VCCP					N17			
		VCCP					R17			
		VCCP					T8			
		VCCP					U11			
		VCCP					U15			
		VCCP					U9			
		VCCA_FPLL					P18			
		VCCA_FPLL					R7			
		VCCA_FPLL					M18			
		VCCA_FPLL					N7			
		VCCBAT					K20			
		VCC_AUX					L16			
		VCC_AUX					M10			
		VCC_AUX					T10			
		VCC_AUX					U17			
		VCCD_FPLL					T18			
		VCCD_FPLL					T7			
		VCCD_FPLL					L19			
		VCCD_FPLL					M7			
		VCCA_GXBL0					T20			
		VCCA_GXBL1					M20			
		VCCH_GXBL0					P20			
		VCCH_GXBL1					L20			
		VCCL_GXBL0					P21			
		VCCL_GXBL0					P22			
		VCCL_GXBL1					L21			
		VCCR_GXBL					K22			
		VCCR_GXBL					N21			
		VCCR_GXBL					U21			
		VCCR_GXBL					U22			
		VCCT_GXBL0					R21			
		VCCT_GXBL0					T22			
		VCCT_GXBL1					M21			
		VCCT_GXBL1					M22			
		VCC					M12			
		VCC					M14			
		VCC					M16			
		VCC					N11			
		VCC					N13			
		VCC					N14			
		VCC					N15			
		VCC					N9			
		VCC					P10			
		VCC					P14			
		VCC					P16			
		VCC					P8			
		VCC					R10			
		VCC					R11			
		VCC					R13			
		VCC					R14			
		VCC					R15			
		VCC					R9			
		VCC					T12			
		VCC					T16			
		VCC					P12			
		VCCIO3A					AA20			
		VCCIO3A					AD21			
		VCCIO3A					AF23			
		VCCIO3D					AC16			
		VCCIO3D					AC18			
		VCCIO3D					AF16			
		VCCIO4A					M5			
		VCCIO4A					P4			
		VCCIO4A					U4			
		VCCIO4A					Y1			
		VCCIO4B					AA6			
		VCCIO4B					AD1			
		VCCIO4B					AD4			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCIO4B					Y4			
		VCCIO4C					AC10			
		VCCIO4C					AD7			
		VCCIO4C					AF7			
		VCCIO4C					Y10			
		VCCIO4D					AA12			
		VCCIO4D					AD12			
		VCCIO4D					AF13			
		VCCIO4D					Y15			
		VCCIO7A					F4			
		VCCIO7A					J1			
		VCCIO7A					J4			
		VCCIO7A					L3			
		VCCIO7B					A3			
		VCCIO7B					C4			
		VCCIO7B					C7			
		VCCIO7B					E6			
		VCCIO7C					A10			
		VCCIO7C					C9			
		VCCIO7C					D10			
		VCCIO7C					G10			
		VCCIO7D					A13			
		VCCIO7D					A15			
		VCCIO7D					D13			
		VCCIO7D					D15			
		VCCIO8A					D22			
		VCCIO8A					F22			
		VCCIO8A					H22			
		VCCIO8D					A18			
		VCCIO8D					E18			
		VCCIO8D					H18			
		VCCPD3					V17			
		VCCPD3					V20			
		VCCPD4A					V6			
		VCCPD4A					V7			
		VCCPD4BCD					U8			
		VCCPD4BCD					V13			
		VCCPD4BCD					V9			
		VCCPD7A					K6			
		VCCPD7A					L7			
		VCCPD7BCD					K10			
		VCCPD7BCD					K13			
		VCCPD7BCD					K8			
		VCCPD8					J19			
		VCCPD8					K16			
		VCCPGM					G6			
		VCCPGM					V21			
		GND					AB11			
		GND					AB14			
		GND					AB17			
		GND					AB2			
		GND					AB20			
		GND					AB5			
		GND					AB8			
		GND					AE11			
		GND					AE14			
		GND					AE17			
		GND					AE2			
		GND					AE20			
		GND					AE22			
		GND					AE5			
		GND					AE8			
		GND					B11			
		GND					B14			
		GND					B17			
		GND					B2			
		GND					B20			
		GND					B23			
		GND					B5			
		GND					B8			
		GND					E11			
		GND					E14			
		GND					E17			
		GND					E2			
		GND					E20			
		GND					E5			
		GND					E8			
		GND					H11			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					H14			
		GND					H17			
		GND					H2			
		GND					H20			
		GND					H5			
		GND					H8			
		GND					L10			
		GND					L14			
		GND					L17			
		GND					L2			
		GND					L5			
		GND					L8			
		GND					M11			
		GND					M13			
		GND					M15			
		GND					M17			
		GND					M9			
		GND					N1			
		GND					N10			
		GND					N16			
		GND					N2			
		GND					N5			
		GND					N8			
		GND					P11			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P9			
		GND					R1			
		GND					R12			
		GND					R16			
		GND					R8			
		GND					T11			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T2			
		GND					T5			
		GND					T9			
		GND					U7			
		GND					W11			
		GND					W14			
		GND					W17			
		GND					W19			
		GND					W2			
		GND					W5			
		GND					W8			
		GND					N12			

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		DNU					E29			
		DNU					F29			
		RREF_TL					F30			
GXB_L1		GXB_TX_L8n					G27			
GXB_L1		GXB_TX_L8p					G28			
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					H30			
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					H29			
GXB_L1		GXB_TX_L7n					J27			
GXB_L1		GXB_TX_L7p					J28			
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					K30			
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					K29			
GXB_L1		GXB_TX_L6n					L27			
GXB_L1		GXB_TX_L6p					L28			
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					M30			
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					M29			
GXB_L1		REFCLK2Ln					R23			
GXB_L1		REFCLK2Lp					R22			
GXB_L0		REFCLK1Ln					U23			
GXB_L0		REFCLK1Lp					U22			
GXB_L0		GXB_TX_L5n					N27			
GXB_L0		GXB_TX_L5p					N28			
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					P30			
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					P29			
GXB_L0		GXB_TX_L4n					R27			
GXB_L0		GXB_TX_L4p					R28			
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					T30			
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					T29			
GXB_L0		GXB_TX_L3n					U27			
GXB_L0		GXB_TX_L3p					U28			
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					V30			
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					V29			
GXB_L0		GXB_TX_L2n					W27			
GXB_L0		GXB_TX_L2p					W28			
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y30			
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y29			
GXB_L0		GXB_TX_L1n					AA27			
GXB_L0		GXB_TX_L1p					AA28			
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB30			
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB29			
GXB_L0		GXB_TX_L0n					AC27			
GXB_L0		GXB_TX_L0p					AC28			
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD30			
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD29			
GXB_L0		REFCLK0Ln					W23			
GXB_L0		REFCLK0Lp					W22			
		DNU					AB26			
3A		TDO		TDO			AF30			
3A		TMS		TMS			AG30			
3A		TCK		TCK			AG29			
3A		TDI		TDI			AF29			
3A		DCLK		DCLK			AJ29			
3A		nCSO		DATA4			AA25			
3A		AS_DATA3		DATA3			AH30			
3A		AS_DATA2		DATA2			AJ30			
3A		AS_DATA1		DATA1			AK29			
3A		AS_DATA0,ASDO		DATA0			AK28			
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AF28			
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AG28	DQ1B		
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AF27	DQ1B		
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AG27	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AE27			
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AE26	DQ1B		
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AH28	DQSn1B/QK1B		
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AJ28	DQS1B/CQ1B/CQn1B/QKn1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AJ27			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AK27	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AB25	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AC25	DQ1B		
3A	VREFB3AN0	IO	VREFB3AN0				AD25			
3A	VREFB3AN0	IO					AE25	DQ1B		
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AG26	DQ1B		
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AH26	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AK26			
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AK25	DQ2B		
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AF25	DQ2B		
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AG25	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AB23			
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AB24	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AH25	DQSn2B/QK2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AJ25	DQS2B/CQ2B/CQn2B/QKn2B		
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AC24			
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AD24	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AF24	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AG24	DQ2B		

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AD23			
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE23	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AJ24	DQ2B		
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AK24	DQ2B		
3D	VREFB3DN0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AC22			
3D	VREFB3DN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AD22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AA22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AB22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB21			
3D	VREFB3DN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC21	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AG23	DQSn3B/QK3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AH23	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AD21			
3D	VREFB3DN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AE22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AF22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AG22	DQ3B	DQ1B	
3D	VREFB3DN0	IO	VREFB3DN0				AA21			
3D	VREFB3DN0	IO					Y20	DQ3B	DQ1B	
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B60n	DIFFOUT_B60n	AH22	DQ3B	DQ1B	
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B60p	DIFFOUT_B60p	AJ22	DQ3B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AD20			
3D	VREFB3DN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AE20	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B62n	DIFFOUT_B62n	AF21	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B62p	DIFFOUT_B62p	AG21	DQ4B	DQ1B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B63n	DIFFOUT_B63n	AA19			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B63p	DIFFOUT_B63p	AB19	DQ4B	DQ1B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B64n	DIFFOUT_B64n	AG20	DQSn4B/QK4B	DQSn1B/QK1B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B64p	DIFFOUT_B64p	AH20	DQS4B/CQ4B/CQn4B/QKn4B	DQS1B/CQ1B/CQn1B/QKn1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AA20			
3D	VREFB3DN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AB20	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B66n	DIFFOUT_B66n	AJ21	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B66p	DIFFOUT_B66p	AK22	DQ4B	DQ1B	
3D	VREFB3DN0	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AC19			
3D	VREFB3DN0	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AD19	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B68n	DIFFOUT_B68n	AK20	DQ4B	DQ1B	
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B68p	DIFFOUT_B68p	AK21	DQ4B	DQ1B	
		VCCD_FPLL					W15			
		VCCA_FPLL					W16			
		DNU					Y16			
4D	VREFB4DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AJ19			
4D	VREFB4DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AK19	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AF19	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AG19	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AC18			
4D	VREFB4DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AD18	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	AH19	DQSn5B/QK5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AH18	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AA18			
4D	VREFB4DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AB18	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AE18	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AF18	DQ5B	DQ2B	
4D	VREFB4DN0	IO	VREFB4DN0				AD17			
4D	VREFB4DN0	IO					AE17	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AA17	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AB17	DQ5B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AA16			
4D	VREFB4DN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AB16	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AG17	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AH17	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	AC16			
4D	VREFB4DN0	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	AD16	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AJ18	DQSn6B/QK6B	DQSn2B/QK2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AK17	DQS6B/CQ6B/CQn6B/QKn6B	DQS2B/CQ2B/CQn2B/QKn2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF16			
4D	VREFB4DN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AG16	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AA15	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81p	DIFFOUT_B81p	AB15	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_TX_B82n	DIFFOUT_B82n	AC15			
4D	VREFB4DN0	IO			DIFFIO_TX_B82p	DIFFOUT_B82p	AD15	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AJ16	DQ6B	DQ2B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AK16	DQ6B	DQ2B	
4C	VREFB4CN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AA14			
4C	VREFB4CN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AB14	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B85n	DIFFOUT_B85n	AG15	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B85p	DIFFOUT_B85p	AH15	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B86n	DIFFOUT_B86n	AE15			
4C	VREFB4CN0	IO			DIFFIO_TX_B86p	DIFFOUT_B86p	AF15	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AJ15	DQSn7B/QK7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AK14	DQS7B/CQ7B/CQn7B/QKn7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AG14			
4C	VREFB4CN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AH14	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AD13	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AE13	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO	VREFB4CN0				AD14			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4C	VREFB4CN0	IO					AE14	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AH13	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AJ13	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AC13			
4C	VREFB4CN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AD12	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AF12	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AF13	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AA13			
4C	VREFB4CN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AB13	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AG12	DQSn8B/QK8B	DQSn3B/QK3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AH12	DQS8B/CQ8B/CQn8B/QKn8B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AJ12			
4C	VREFB4CN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AK12	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AB12	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AC12	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	Y12			
4C	VREFB4CN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	Y13	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AG11	DQ8B	DQ3B	DQ1B
4C	VREFB4CN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AH11	DQ8B	DQ3B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD11			
4B	VREFB4BN0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE11	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B100n	DIFFOUT_B100n	AA12	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B100p	DIFFOUT_B100p	AB11	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B101n	DIFFOUT_B101n	AA11			
4B	VREFB4BN0	IO			DIFFIO_TX_B101p	DIFFOUT_B101p	AA10	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B102n	DIFFOUT_B102n	AK11	DQSn9B/QK9B	DQ4B	DQSn1B/QK1B
4B	VREFB4BN0	IO			DIFFIO_RX_B102p	DIFFOUT_B102p	AK10	DQS9B/CQ9B/CQn9B/QKn9B	DQ4B	DQS1B/CQ1B/CQn1B/QKn1B
4B	VREFB4BN0	IO			DIFFIO_TX_B103n	DIFFOUT_B103n	AF10			
4B	VREFB4BN0	IO			DIFFIO_TX_B103p	DIFFOUT_B103p	AG10	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B104n	DIFFOUT_B104n	AB10	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B104p	DIFFOUT_B104p	AB9	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B105n	DIFFOUT_B105n	AC10			
4B	VREFB4BN0	IO			DIFFIO_TX_B105p	DIFFOUT_B105p	AD10	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B106n	DIFFOUT_B106n	AH9	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B106p	DIFFOUT_B106p	AJ10	DQ9B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AE9			
4B	VREFB4BN0	IO			DIFFIO_TX_B107p	DIFFOUT_B107p	AF9	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B108n	DIFFOUT_B108n	AJ9	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B108p	DIFFOUT_B108p	AK8	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B109n	DIFFOUT_B109n	AC9			
4B	VREFB4BN0	IO			DIFFIO_TX_B109p	DIFFOUT_B109p	AD9	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B110n	DIFFOUT_B110n	AA9	DQSn10B/QK10B	DQSn4B/QK4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B110p	DIFFOUT_B110p	AB8	DQS10B/CQ10B/CQn10B/QKn10B	DQS4B/CQ4B/CQn4B/QKn4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_TX_B111n	DIFFOUT_B111n	AG8			
4B	VREFB4BN0	IO			DIFFIO_TX_B111p	DIFFOUT_B111p	AH8	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B112n	DIFFOUT_B112n	AJ7	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B112p	DIFFOUT_B112p	AK7	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO	VREFB4BN0				AD8			
4B	VREFB4BN0	IO					AE8	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AG7	DQ10B	DQ4B	DQ1B
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AH7	DQ10B	DQ4B	DQ1B
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B114n	DIFFOUT_B114n	AF7			
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B114p	DIFFOUT_B114p	AG6	DQ11B	DQ5B	
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B115n	DIFFOUT_B115n	AJ6	DQ11B	DQ5B	
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B115p	DIFFOUT_B115p	AK6	DQ11B	DQ5B	
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B116n	DIFFOUT_B116n	AA8			
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B116p	DIFFOUT_B116p	AB7	DQ11B	DQ5B	
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B117n	DIFFOUT_B117n	AK5	DQSn11B/QK11B	DQ5B	
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B117p	DIFFOUT_B117p	AK4	DQS11B/CQ11B/CQn11B/QKn11B	DQ5B	
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B118n	DIFFOUT_B118n	AD7			
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B118p	DIFFOUT_B118p	AE7	DQ11B	DQ5B	
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B119n	DIFFOUT_B119n	AA6	DQ11B	DQ5B	
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B119p	DIFFOUT_B119p	AB6	DQ11B	DQ5B	
4A	VREFB4AN0	IO	VREFB4AN0				AC6			
4A	VREFB4AN0	IO					AC7	DQ11B	DQ5B	
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B120n	DIFFOUT_B120n	AE6	DQ11B	DQ5B	
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B120p	DIFFOUT_B120p	AF6	DQ11B	DQ5B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B121n	DIFFOUT_B121n	AG5			
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B121p	DIFFOUT_B121p	AH5	DQ12B	DQ5B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B122n	DIFFOUT_B122n	AH4	DQ12B	DQ5B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B122p	DIFFOUT_B122p	AJ4	DQ12B	DQ5B	
4A	VREFB4AN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AD6			
4A	VREFB4AN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AE5	DQ12B	DQ5B	
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B124n	DIFFOUT_B124n	AJ3	DQSn12B/QK12B	DQSn5B/QK5B	
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B124p	DIFFOUT_B124p	AK3	DQS12B/CQ12B/CQn12B/QKn12B	DQS5B/CQ5B/CQn5B/QKn5B	
4A	VREFB4AN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AG4			
4A	VREFB4AN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AG3	DQ12B	DQ5B	
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B126n	DIFFOUT_B126n	AJ1	DQ12B	DQ5B	
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B126p	DIFFOUT_B126p	AK2	DQ12B	DQ5B	
4A	VREFB4AN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AE4			
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B127p	DIFFOUT_B127p	AF4	DQ12B	DQ5B	
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B128n	DIFFOUT_B128n	AH2	DQ12B	DQ5B	
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B128p	DIFFOUT_B128p	AH1	DQ12B	DQ5B	
		RREF_BR					AF1			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		DNU					AF2			
		DNU					AG2			
		GND					W9			
		GND					W8			
		GND					AD2			
		GND					AD1			
		DNU					AC3			
		DNU					AC4			
		GND					AB2			
		GND					AB1			
		DNU					AA3			
		DNU					AA4			
		GND					Y2			
		GND					Y1			
		DNU					W3			
		DNU					W4			
		GND					U9			
		GND					U8			
		GND					V2			
		GND					V1			
		DNU					U3			
		DNU					U4			
		GND					T2			
		GND					T1			
		DNU					R3			
		DNU					R4			
		GND					P2			
		GND					P1			
		DNU					N3			
		DNU					N4			
		GND					M2			
		GND					M1			
		DNU					L3			
		DNU					L4			
		GND					K2			
		GND					K1			
		DNU					J3			
		DNU					J4			
		GND					H2			
		GND					H1			
		DNU					G3			
		DNU					G4			
		GND					R9			
		GND					R8			
		DNU					H5			
		GND					F5			
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E1	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	F1	DQ1T	DQ1T	
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	E4	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	E3			
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D2	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	D1	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	D4	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	D3			
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	A2	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T	
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	B1	DQSn1T/QK1T	DQSn1T/QK1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C2	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	C1			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	A3	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	B3	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	B4	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	C4			
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	C5	DQ2T	DQ1T	
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	D5	DQ2T	DQ1T	
7A	VREFB7AN0	IO					J6	DQ2T	DQ1T	
7A	VREFB7AN0	IO	VREFB7AN0				K6			
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	A5	DQ2T	DQ1T	
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	A4	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFOUT_T11p	J7	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T11n	DIFFOUT_T11n	K7			
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	D6	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	E6	DQSn2T/QK2T	DQ1T	
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	G6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	H6			
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	A6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	B6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	G7	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	H7			
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	F8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	G8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO					J8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO	VREFB7BN0				K8			
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	E7	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	F7	DQ3T	DQ2T	DQ1T

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7B	VREFB7BN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	G9	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	H9			
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	A7	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	A8	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B7	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C7			
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	C8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	D8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J9	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	K9			
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D9	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	E9	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	B10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	B9			
7B	VREFB7BN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	A11	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	A10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K10			
7B	VREFB7BN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C10	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS1T/CQ1T/CQn1T/QKn1T
7B	VREFB7BN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D10	DQSn4T/QK4T	DQ2T	DQSn1T/QK1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	E10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F10			
7B	VREFB7BN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	C11	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	D11	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	G10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	H10			
7C	VREFB7CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	J11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	K11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	F11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	G11			
7C	VREFB7CN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	B13	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	B12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	D12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	E12			
7C	VREFB7CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	J12	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	K12	DQSn5T/QK5T	DQSn3T/QK3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	G12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	H12			
7C	VREFB7CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	C13	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	D13	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E13	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	F13			
7C	VREFB7CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	J14	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	K14	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO					J13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO	VREFB7CN0				K13			
7C	VREFB7CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	A14	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	A13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	F14	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	G14			
7C	VREFB7CN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	C14	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	D14	DQSn6T/QK6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	G13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	H13			
7C	VREFB7CN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	A15	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	B15	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	D15	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	E15			
7D	VREFB7DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	F15	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	G15	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	J16	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	K16			
7D	VREFB7DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	H15	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	J15	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	D16	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	E16			
7D	VREFB7DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	B16	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	C16	DQSn7T/QK7T	DQSn4T/QK4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	G16	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	H16			
7D	VREFB7DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	A17	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	A16	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	C17	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	D17			
7D	VREFB7DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	J17	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	K17	DQ8T	DQ4T	
7D	VREFB7DN0	IO					J18	DQ8T	DQ4T	
7D	VREFB7DN0	IO	VREFB7DN0				K18			
7D	VREFB7DN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	D18	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	E18	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F17	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	G17			
7D	VREFB7DN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	B18	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	C19	DQSn8T/QK8T	DQ4T	

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7D	VREFB7DN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	G18	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	H18			
7D	VREFB7DN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	A19	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	B19	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	D19	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	E19			
		VCCA_FPLL					M16			
		VCCD_FPLL					M15			
		DNU					K15			
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	F19	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	G20	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	J19	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	K19			
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	J20	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	K20	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	F20	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	F21			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	C20	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	D20	DQSn9T/QK9T	DQSn5T/QK5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	G19	DQ9T	DQ5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	H19			
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T67p	DIFFOUT_T67p	A21	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T67n	DIFFOUT_T67n	B21	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	D21	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	E21			
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T69p	DIFFOUT_T69p	D22	DQ10T	DQ5T	
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T69n	DIFFOUT_T69n	E22	DQ10T	DQ5T	
8D	VREFB8DN0	IO					J21	DQ10T	DQ5T	
8D	VREFB8DN0	IO	VREFB8DN0				K21			
8D	VREFB8DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	J22	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	K22	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T71p	DIFFOUT_T71p	G22	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T71n	DIFFOUT_T71n	H22			
8D	VREFB8DN0	IO			DIFFIO_RX_T72p	DIFFOUT_T72p	B22	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T72n	DIFFOUT_T72n	C22	DQSn10T/QK10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T73p	DIFFOUT_T73p	G21	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T73n	DIFFOUT_T73n	H21			
8D	VREFB8DN0	IO			DIFFIO_RX_T74p	DIFFOUT_T74p	F23	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T74n	DIFFOUT_T74n	G23	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T75p	DIFFOUT_T75p	C23	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T75n	DIFFOUT_T75n	D23			
8A	VREFB8AN0	IO			DIFFIO_RX_T114p	DIFFOUT_T114p	A23	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_RX_T114n	DIFFOUT_T114n	A24	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	L22	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T115n	DIFFOUT_T115n	K23			
8A	VREFB8AN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	D24	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	E24	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T117p	DIFFOUT_T117p	B24	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T117n	DIFFOUT_T117n	B25			
8A	VREFB8AN0	IO			DIFFIO_RX_T118p	DIFFOUT_T118p	A26	DQS11T/CQ11T/CQn11T/QKn11T		
8A	VREFB8AN0	IO			DIFFIO_RX_T118n	DIFFOUT_T118n	A27	DQSn11T/QK11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T119p	DIFFOUT_T119p	K24	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T119n	DIFFOUT_T119n	J23			
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T120p	DIFFOUT_T120p	C25	DQ11T		
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T120n	DIFFOUT_T120n	D25	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T121p	DIFFOUT_T121p	J25	DQ11T		
8A	VREFB8AN0	IO			DIFFIO_TX_T121n	DIFFOUT_T121n	K25			
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T122p	DIFFOUT_T122p	D26	DQ12T		
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T122n	DIFFOUT_T122n	E25	DQ12T		
8A	VREFB8AN0	IO					G24	DQ12T		
8A	VREFB8AN0	IO	VREFB8AN0				H25			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T123p	DIFFOUT_T123p	C27	DQ12T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T123n	DIFFOUT_T123n	C26	DQ12T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T124p	DIFFOUT_T124p	A28	DQ12T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T124n	DIFFOUT_T124n	B27			
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T125p	DIFFOUT_T125p	A29	DQS12T/CQ12T/CQn12T/QKn12T		
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T125n	DIFFOUT_T125n	B28	DQSn12T/QK12T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	H24	DQ12T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	J24			
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T127p	DIFFOUT_T127p	C28	DQ12T		
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T127n	DIFFOUT_T127n	D27	DQ12T		
8A	VREFB8AN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	F25	DQ12T		
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T128n	DIFFOUT_T128n	G25			
8A		MSEL0		MSEL0			C30			
8A		MSEL1		MSEL1			D30			
8A		MSEL2		MSEL2			C29			
8A		MSEL3		MSEL3			D29			
8A		MSEL4		MSEL4			F26			
8A		CONF_DONE		CONF_DONE			B30			
8A		nSTATUS		nSTATUS			D28			
8A		nCE		nCE			E28			
8A		nCONFIG		nCONFIG			E27			
		GND					H26			
		GND					AA26			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AA29			
		GND					AA30			
		GND					AB27			
		GND					AB28			
		GND					AC26			
		GND					AC29			
		GND					AC30			
		GND					AD27			
		GND					AD28			
		GND					AE28			
		GND					AE29			
		GND					AE30			
		GND					E30			
		GND					F27			
		GND					F28			
		GND					G26			
		GND					G29			
		GND					G30			
		GND					H27			
		GND					H28			
		GND					J26			
		GND					J29			
		GND					J30			
		GND					K27			
		GND					K28			
		GND					L25			
		GND					L26			
		GND					L29			
		GND					L30			
		GND					M24			
		GND					M27			
		GND					M28			
		GND					N23			
		GND					N24			
		GND					N26			
		GND					N29			
		GND					N30			
		GND					P23			
		GND					P25			
		GND					P27			
		GND					P28			
		GND					R24			
		GND					R29			
		GND					R30			
		GND					T23			
		GND					T27			
		GND					T28			
		GND					U24			
		GND					U26			
		GND					U29			
		GND					U30			
		GND					V23			
		GND					V25			
		GND					V27			
		GND					V28			
		GND					W24			
		GND					W29			
		GND					W30			
		GND					Y22			
		GND					Y23			
		GND					Y24			
		GND					Y25			
		GND					Y26			
		GND					Y27			
		GND					Y28			
		GND					AA1			
		GND					AA2			
		GND					AA5			
		GND					AB3			
		GND					AB4			
		GND					AC1			
		GND					AC2			
		GND					AC5			
		GND					AD3			
		GND					AD4			
		GND					AE1			
		GND					AE2			
		GND					AE3			
		GND					AG1			
		GND					F3			
		GND					F4			
		GND					G1			
		GND					G2			
		GND					G5			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					H3			
		GND					H4			
		GND					J1			
		GND					J2			
		GND					J5			
		GND					K3			
		GND					K4			
		GND					L1			
		GND					L2			
		GND					L5			
		GND					L6			
		GND					M3			
		GND					M4			
		GND					M7			
		GND					N1			
		GND					N2			
		GND					N5			
		GND					N8			
		GND					N9			
		GND					P3			
		GND					P4			
		GND					P6			
		GND					P8			
		GND					R1			
		GND					R2			
		GND					R5			
		GND					R7			
		GND					T3			
		GND					T4			
		GND					T8			
		GND					U1			
		GND					U2			
		GND					U5			
		GND					U7			
		GND					V3			
		GND					V4			
		GND					V6			
		GND					V8			
		GND					W1			
		GND					W2			
		GND					W7			
		GND					Y3			
		GND					Y4			
		GND					Y5			
		GND					Y6			
		GND					Y7			
		GND					Y8			
		GND					Y9			
		VCCP					L11			
		VCCP					L15			
		VCCP					L19			
		VCCP					L20			
		VCCP					L9			
		VCCP					W11			
		VCCP					W13			
		VCCP					W17			
		VCCP					W19			
		VCCP					W21			
		VCCA_FPLL					T22			
		VCCA_FPLL					T9			
		VCCA_FPLL					P22			
		VCCA_FPLL					P9			
		VCCBAT					K26			
		VCC_AUX					M12			
		VCC_AUX					M18			
		VCC_AUX					W12			
		VCC_AUX					W18			
		VCCD_FPLL					V22			
		VCCD_FPLL					V9			
		VCCD_FPLL					N22			
		VCCD_FPLL					M8			
		VCCA_GXBL0					V24			
		VCCA_GXBR0					V7			
		VCCA_GXBL1					P24			
		VCCA_GXBR1					P7			
		VCCH_GXBL0					T24			
		VCCH_GXBR0					T7			
		VCCH_GXBL1					N25			
		VCCH_GXBR1					N7			
		VCCL_GXBL0					T25			
		VCCL_GXBL0					T26			
		VCCL_GXBR0					U6			
		VCCL_GXBL1					M25			
		VCCL_GXBR1					M6			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCL_GXBR1					N6			
		VCCR_GXBL					M26			
		VCCR_GXBL					R25			
		VCCR_GXBL					R26			
		VCCR_GXBL					W25			
		VCCR_GXBL					W26			
		VCCR_GXBR					M5			
		VCCR_GXBR					T5			
		VCCR_GXBR					T6			
		VCCR_GXBR					W5			
		VCCR_GXBR					W6			
		VCCT_GXBL0					U25			
		VCCT_GXBL0					V26			
		VCCT_GXBR0					V5			
		VCCT_GXBL1					P26			
		VCCT_GXBR1					P5			
		VCCT_GXBR1					R6			
		VCC					M10			
		VCC					M14			
		VCC					M20			
		VCC					N11			
		VCC					N13			
		VCC					N15			
		VCC					N17			
		VCC					N19			
		VCC					N21			
		VCC					P10			
		VCC					P12			
		VCC					P14			
		VCC					P16			
		VCC					P18			
		VCC					P20			
		VCC					R11			
		VCC					R13			
		VCC					R15			
		VCC					R17			
		VCC					R19			
		VCC					R21			
		VCC					T10			
		VCC					T12			
		VCC					T14			
		VCC					T18			
		VCC					T20			
		VCC					U11			
		VCC					U13			
		VCC					U15			
		VCC					U17			
		VCC					U19			
		VCC					U21			
		VCC					V10			
		VCC					V12			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					T16			
		VCCIO3A					AD26			
		VCCIO3A					AE24			
		VCCIO3A					AH24			
		VCCIO3A					AH27			
		VCCIO3D					AE19			
		VCCIO3D					AE21			
		VCCIO3D					AH21			
		VCCIO3D					AK23			
		VCCIO4A					AB5			
		VCCIO4A					AD5			
		VCCIO4A					AH3			
		VCCIO4A					AH6			
		VCCIO4B					AE10			
		VCCIO4B					AG9			
		VCCIO4B					AH10			
		VCCIO4B					AK9			
		VCCIO4C					AE12			
		VCCIO4C					AG13			
		VCCIO4C					AK13			
		VCCIO4C					AK15			
		VCCIO4D					AE16			
		VCCIO4D					AG18			
		VCCIO4D					AH16			
		VCCIO4D					AK18			
		VCCIO7A					C3			
		VCCIO7A					C6			
		VCCIO7A					F2			
		VCCIO7A					F6			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCIO7B					A9			
		VCCIO7B					C9			
		VCCIO7B					D7			
		VCCIO7B					F9			
		VCCIO7C					A12			
		VCCIO7C					C12			
		VCCIO7C					C15			
		VCCIO7C					F12			
		VCCIO7D					A18			
		VCCIO7D					C18			
		VCCIO7D					F16			
		VCCIO7D					F18			
		VCCIO8A					A25			
		VCCIO8A					C24			
		VCCIO8A					F24			
		VCCIO8A					L23			
		VCCIO8D					A20			
		VCCIO8D					A22			
		VCCIO8D					C21			
		VCCIO8D					F22			
		VCCPD3					AA23			
		VCCPD3					Y21			
		VCCPD4A					AA7			
		VCCPD4BCD					Y10			
		VCCPD4BCD					Y15			
		VCCPD4BCD					Y18			
		VCCPD7A					L8			
		VCCPD7BCD					L13			
		VCCPD7BCD					L17			
		VCCPD7BCD					M9			
		VCCPD8					M22			
		VCCPD8					M23			
		VCCPGM					K5			
		VCCPGM					AA24			
		GND					AC11			
		GND					AC14			
		GND					AC17			
		GND					AC20			
		GND					AC23			
		GND					AC8			
		GND					AF11			
		GND					AF14			
		GND					AF17			
		GND					AF20			
		GND					AF23			
		GND					AF26			
		GND					AF3			
		GND					AF5			
		GND					AF8			
		GND					AH29			
		GND					AJ11			
		GND					AJ14			
		GND					AJ17			
		GND					AJ2			
		GND					AJ20			
		GND					AJ23			
		GND					AJ26			
		GND					AJ5			
		GND					AJ8			
		GND					B11			
		GND					B14			
		GND					B17			
		GND					B2			
		GND					B20			
		GND					B23			
		GND					B26			
		GND					B29			
		GND					B5			
		GND					B8			
		GND					E11			
		GND					E14			
		GND					E17			
		GND					E2			
		GND					E20			
		GND					E23			
		GND					E26			
		GND					E5			
		GND					E8			
		GND					H11			
		GND					H14			
		GND					H17			
		GND					H20			
		GND					H23			
		GND					H8			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					L10			
		GND					L12			
		GND					L14			
		GND					L16			
		GND					L18			
		GND					L21			
		GND					L24			
		GND					L7			
		GND					M11			
		GND					M13			
		GND					M17			
		GND					M19			
		GND					M21			
		GND					N10			
		GND					N12			
		GND					N14			
		GND					N16			
		GND					N18			
		GND					N20			
		GND					P11			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P19			
		GND					P21			
		GND					R10			
		GND					R12			
		GND					R14			
		GND					R18			
		GND					R20			
		GND					T11			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					U10			
		GND					U12			
		GND					U14			
		GND					U16			
		GND					U18			
		GND					U20			
		GND					V11			
		GND					V13			
		GND					V15			
		GND					V17			
		GND					V19			
		GND					V21			
		GND					W10			
		GND					W14			
		GND					W20			
		GND					Y11			
		GND					Y14			
		GND					Y17			
		GND					Y19			
		GND					R16			

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		DNU					E33			
		DNU					F33			
		RREF_TL					F34			
		GND					R27			
		GND					R26			
		DNU					G31			
		DNU					G32			
		GND					H34			
		GND					H33			
		DNU					J31			
		DNU					J32			
		GND					K34			
		GND					K33			
		DNU					L31			
		DNU					L32			
		GND					M34			
		GND					M33			
GXB_L1		GXB_TX_L8n					N31			
GXB_L1		GXB_TX_L8p					N32			
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					P34			
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					P33			
GXB_L1		GXB_TX_L7n					R31			
GXB_L1		GXB_TX_L7p					R32			
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					T34			
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					T33			
GXB_L1		GXB_TX_L6n					U31			
GXB_L1		GXB_TX_L6p					U32			
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					V34			
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					V33			
GXB_L1		REFCLK2Ln					U27			
GXB_L1		REFCLK2Lp					U26			
GXB_L0		REFCLK1Ln					W27			
GXB_L0		REFCLK1Lp					W26			
GXB_L0		GXB_TX_L5n					W31			
GXB_L0		GXB_TX_L5p					W32			
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					Y34			
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					Y33			
GXB_L0		GXB_TX_L4n					AA31			
GXB_L0		GXB_TX_L4p					AA32			
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AB34			
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AB33			
GXB_L0		GXB_TX_L3n					AC31			
GXB_L0		GXB_TX_L3p					AC32			
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AD34			
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AD33			
GXB_L0		GXB_TX_L2n					AE31			
GXB_L0		GXB_TX_L2p					AE32			
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AF34			
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AF33			
GXB_L0		GXB_TX_L1n					AG31			
GXB_L0		GXB_TX_L1p					AG32			
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AH34			
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AH33			
GXB_L0		GXB_TX_L0n					AJ31			
GXB_L0		GXB_TX_L0p					AJ32			
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AK34			
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AK33			
GXB_L0		REFCLK0Ln					AA28			
GXB_L0		REFCLK0Lp					AA27			
		DNU					AL32			
3A		TDO		TDO			AC28			
3A		TMS		TMS			AF30			
3A		TCK		TCK			AN32			
3A		TDI		TDI			AC29			
3A		DCLK		DCLK			AM32			
3A		nCSO		DATA4			AM34			
3A		AS_DATA3		DATA3			AM33			
3A		AS_DATA2		DATA2			AP33			
3A		AS_DATA1		DATA1			AN33			
3A		AS_DATA0,ASDO		DATA0			AN34			
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AL31			
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AM31	DQ1B		
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AP31	DQ1B		
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AP32	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AD27			
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AD26	DQ1B		
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ29	DQSn1B/QK1B		
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK29	DQS1B/CQ1B/CQn1B/QKn1B		

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AL30			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AM30	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AN30	DQ1B		
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AP30	DQ1B		
3A	VREFB3AN0	IO	VREFB3AN0				AE27			
3A	VREFB3AN0	IO					AF28	DQ1B		
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AH28	DQ1B		
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AJ28	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AL29			
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AM29	DQ2B	DQ1B	
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AN29	DQ2B	DQ1B	
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AP29	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AE29			
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AF29	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AG27	DQSn2B/QK2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AH27	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AL28			
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AM28	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AP27	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AP28	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AG29			
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AH29	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AK27	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AL27	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AG26			
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AH26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AJ26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AK26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AD29			
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AE28	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AL26	DQSn3B/QK3B	DQSn1B/QK1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AM26	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AN27			
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AN26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AP25	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AP26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AE26			
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AF26	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AL25	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AM25	DQ3B	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AE23			
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AC24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AC25	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AA25			
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AB25	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AD24	DQSn4B/QK4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AE25	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AF25			
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AG24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AH24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AH25	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	VREFB3BN0				Y23			
3B	VREFB3BN0	IO					AB24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AJ25	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AK24	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AK23			
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AL24	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AF23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AG23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC23			
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AH23	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ23	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AL23			
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AN23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AN24	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA23			
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AP22	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ5B	DQ2B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AE21			
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AE22	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AL21	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AL22	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22			
3C	VREFB3CN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC22	DQ6B	DQ3B	DQ1B

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3C	VREFB3CN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AH21	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B
3C	VREFB3CN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AH22	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AF22			
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AG21	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AJ22	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AK21	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AA21			
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AB21	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AM22	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AN21	DQ6B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AC21			
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AD21	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AP20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AA20			
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AL20	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AM20	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AJ20			
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AK20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AG20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AH20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO	VREFB3CN0				AC20			
3C	VREFB3CN0	IO					AD20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AE20	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AF20	DQ7B	DQ3B	DQ1B
3D	VREFB3DN0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AH19			
3D	VREFB3DN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AJ19	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AL19	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AM19	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB19			
3D	VREFB3DN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC19	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AN18	DQSn8B/QK8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AP19	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AE19			
3D	VREFB3DN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AF19	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AK18	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AL18	DQ8B	DQ4B	
3D	VREFB3DN0	IO	VREFB3DN0				AB18			
3D	VREFB3DN0	IO					AA18	DQ8B	DQ4B	
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B60n	DIFFOUT_B60n	AG18	DQ8B	DQ4B	
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B60p	DIFFOUT_B60p	AH18	DQ8B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AN17			
3D	VREFB3DN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AP17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B62n	DIFFOUT_B62n	AG17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B62p	DIFFOUT_B62p	AH17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B63n	DIFFOUT_B63n	AA17			
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B63p	DIFFOUT_B63p	AB17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B64n	DIFFOUT_B64n	AJ17	DQSn9B/QK9B	DQSn4B/QK4B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B64p	DIFFOUT_B64p	AK17	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B	
3D	VREFB3DN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AL17			
3D	VREFB3DN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AM17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B66n	DIFFOUT_B66n	AE17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B66p	DIFFOUT_B66p	AF17	DQ9B	DQ4B	
3D	VREFB3DN0	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AC17			
3D	VREFB3DN0	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AC18	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B68n	DIFFOUT_B68n	AD17	DQ9B	DQ4B	
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B68p	DIFFOUT_B68p	AE18	DQ9B	DQ4B	
		VCCD_FPLL					Y17			
		VCCA_FPLL					Y18			
		DNU					AD18			
4D	VREFB4DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AP16			
4D	VREFB4DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AN15	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AH16	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AJ16	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AE16			
4D	VREFB4DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AF16	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	Y15	DQSn10B/QK10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AA15	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AB16			
4D	VREFB4DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AC16	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AL16	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AM16	DQ10B	DQ5B	
4D	VREFB4DN0	IO	VREFB4DN0				AJ14			
4D	VREFB4DN0	IO					AK14	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AL14	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AM14	DQ10B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AA14			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4D	VREFB4DN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AB15	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AK15	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AL15	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	AG14			
4D	VREFB4DN0	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	AH14	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AG15	DQSn11B/QK11B	DQSn5B/QK5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AH15	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AD15			
4D	VREFB4DN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AE15	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AE14	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B81p	DIFFOUT_B81p	AF14	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_TX_B82n	DIFFOUT_B82n	AB14			
4D	VREFB4DN0	IO			DIFFIO_TX_B82p	DIFFOUT_B82p	AC15	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AC14	DQ11B	DQ5B	
4D	VREFB4DN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AD14	DQ11B	DQ5B	
4C	VREFB4CN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AB13			
4C	VREFB4CN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AC13	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B85n	DIFFOUT_B85n	AN14	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B85p	DIFFOUT_B85p	AP14	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B86n	DIFFOUT_B86n	AN12			
4C	VREFB4CN0	IO			DIFFIO_TX_B86p	DIFFOUT_B86p	AP13	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AL13	DQSn12B/QK12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AM13	DQS12B/CQ12B/CQn12B/QKn12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	Y11			
4C	VREFB4CN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AA12	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AK12	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AL12	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO	VREFB4CN0				AK11			
4C	VREFB4CN0	IO					AL11	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AH13	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AJ13	DQ12B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AB11			
4C	VREFB4CN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AB12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AG12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AH12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AH11			
4C	VREFB4CN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AJ11	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AE13	DQSn13B/QK13B	DQSn6B/QK6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AF13	DQS13B/CQ13B/CQn13B/QKn13B	DQS6B/CQ6B/CQn6B/QKn6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AC11			
4C	VREFB4CN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AC12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AD12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AE12	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AD11			
4C	VREFB4CN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AE11	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AF11	DQ13B	DQ6B	DQ2B
4C	VREFB4CN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AG11	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD9			
4B	VREFB4BN0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE9	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B100n	DIFFOUT_B100n	AM11	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B100p	DIFFOUT_B100p	AN11	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B101n	DIFFOUT_B101n	AL10			
4B	VREFB4BN0	IO			DIFFIO_TX_B101p	DIFFOUT_B101p	AM10	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B102n	DIFFOUT_B102n	AP10	DQSn14B/QK14B	DQ7B	DQSn2B/QK2B
4B	VREFB4BN0	IO			DIFFIO_RX_B102p	DIFFOUT_B102p	AP11	DQS14B/CQ14B/CQn14B/QKn14B	DQ7B	DQS2B/CQ2B/CQn2B/QKn2B
4B	VREFB4BN0	IO			DIFFIO_TX_B103n	DIFFOUT_B103n	AA10			
4B	VREFB4BN0	IO			DIFFIO_TX_B103p	DIFFOUT_B103p	AB10	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B104n	DIFFOUT_B104n	AH10	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B104p	DIFFOUT_B104p	AJ10	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B105n	DIFFOUT_B105n	AK9			
4B	VREFB4BN0	IO			DIFFIO_TX_B105p	DIFFOUT_B105p	AL9	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B106n	DIFFOUT_B106n	AN9	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B106p	DIFFOUT_B106p	AN8	DQ14B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AC9			
4B	VREFB4BN0	IO			DIFFIO_TX_B107p	DIFFOUT_B107p	AC10	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B108n	DIFFOUT_B108n	AG9	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B108p	DIFFOUT_B108p	AH9	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B109n	DIFFOUT_B109n	AE10			
4B	VREFB4BN0	IO			DIFFIO_TX_B109p	DIFFOUT_B109p	AF10	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B110n	DIFFOUT_B110n	AL8	DQSn15B/QK15B	DQSn7B/QK7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B110p	DIFFOUT_B110p	AM8	DQS15B/CQ15B/CQn15B/QKn15B	DQS7B/CQ7B/CQn7B/QKn7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B111n	DIFFOUT_B111n	AC8			
4B	VREFB4BN0	IO			DIFFIO_TX_B111p	DIFFOUT_B111p	AD8	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B112n	DIFFOUT_B112n	AJ8	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B112p	DIFFOUT_B112p	AK8	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO	VREFB4BN0				AE8			
4B	VREFB4BN0	IO					AF8	DQ15B	DQ7B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AG8	DQ15B	DQ7B	DQ2B

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AH8	DQ15B	DQ7B	DQ2B
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B114n	DIFFOUT_B114n	AP8			
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B114p	DIFFOUT_B114p	AP7	DQ16B	DQ8B	
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B115n	DIFFOUT_B115n	AL7	DQ16B	DQ8B	
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B115p	DIFFOUT_B115p	AM7	DQ16B	DQ8B	
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B116n	DIFFOUT_B116n	AM6			
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B116p	DIFFOUT_B116p	AN6	DQ16B	DQ8B	
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B117n	DIFFOUT_B117n	AP6	DQSn16B/QK16B	DQ8B	
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B117p	DIFFOUT_B117p	AP5	DQS16B/CQ16B/CQn16B/QKn16B	DQ8B	
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B118n	DIFFOUT_B118n	AE7			
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B118p	DIFFOUT_B118p	AF7	DQ16B	DQ8B	
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B119n	DIFFOUT_B119n	AM5	DQ16B	DQ8B	
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B119p	DIFFOUT_B119p	AN5	DQ16B	DQ8B	
4A	VREFB4AN0	IO	VREFB4AN0				AK6			
4A	VREFB4AN0	IO					AL6	DQ16B	DQ8B	
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B120n	DIFFOUT_B120n	AH7	DQ16B	DQ8B	
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B120p	DIFFOUT_B120p	AJ7	DQ16B	DQ8B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B121n	DIFFOUT_B121n	AD6			
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B121p	DIFFOUT_B121p	AE6	DQ17B	DQ8B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B122n	DIFFOUT_B122n	AP3	DQ17B	DQ8B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B122p	DIFFOUT_B122p	AP4	DQ17B	DQ8B	
4A	VREFB4AN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AH6			
4A	VREFB4AN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AJ6	DQ17B	DQ8B	
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B124n	DIFFOUT_B124n	AP2	DQSn17B/QK17B	DQSn8B/QK8B	
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B124p	DIFFOUT_B124p	AN3	DQS17B/CQ17B/CQn17B/QKn17B	DQS8B/CQ8B/CQn8B/QKn8B	
4A	VREFB4AN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AC7			
4A	VREFB4AN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AC6	DQ17B	DQ8B	
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B126n	DIFFOUT_B126n	AL4	DQ17B	DQ8B	
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B126p	DIFFOUT_B126p	AL5	DQ17B	DQ8B	
4A	VREFB4AN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AM3			
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B127p	DIFFOUT_B127p	AM4	DQ17B	DQ8B	
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B128n	DIFFOUT_B128n	AF6	DQ17B	DQ8B	
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B128p	DIFFOUT_B128p	AG6	DQ17B	DQ8B	
		RREF_BR					AM1			
		DNU					AM2			
		DNU					AN2			
		GND					AA8			
		GND					AA7			
		GND					AK2			
		GND					AK1			
		DNU					AJ3			
		DNU					AJ4			
		GND					AH2			
		GND					AH1			
		DNU					AG3			
		DNU					AG4			
		GND					AF2			
		GND					AF1			
		DNU					AE3			
		DNU					AE4			
		GND					AD2			
		GND					AD1			
		DNU					AC3			
		DNU					AC4			
		GND					AB2			
		GND					AB1			
		DNU					AA3			
		DNU					AA4			
		GND					Y2			
		GND					Y1			
		DNU					W3			
		DNU					W4			
		GND					W9			
		GND					W8			
		GND					U9			
		GND					U8			
		GND					V2			
		GND					V1			
		DNU					U3			
		DNU					U4			
		GND					T2			
		GND					T1			
		DNU					R3			
		DNU					R4			
		GND					P2			
		GND					P1			
		DNU					N3			
		DNU					N4			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					M2			
		GND					M1			
		DNU					L3			
		DNU					L4			
		GND					K2			
		GND					K1			
		DNU					J3			
		DNU					J4			
		GND					H2			
		GND					H1			
		DNU					G3			
		DNU					G4			
		GND					R9			
		GND					R8			
		DNU					K5			
		GND					H5			
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E3	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	E4	DQ1T	DQ1T	
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	E1	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	F1			
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D1	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	E2	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	G6	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	H6			
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	C1	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T	
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	C2	DQSn1T/QK1T	DQSn1T/QK1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	E5	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	F6			
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	C3	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	D3	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J6	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K6			
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	A3	DQ2T	DQ1T	
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	B3	DQ2T	DQ1T	
7A	VREFB7AN0	IO					L6	DQ2T	DQ1T	
7A	VREFB7AN0	IO	VREFB7AN0				M7			
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	C6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	D5	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFOUT_T11p	A2	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T11n	DIFFOUT_T11n	B2			
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	B5	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	C4	DQSn2T/QK2T	DQ1T	
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	A5	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	A4			
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	D6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	E6	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	J7	DQ2T	DQ1T	
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	K7			
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	K9	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	K8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO					M10	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO	VREFB7BN0				P11			
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	C8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	D7	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	E8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	F7			
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	N10	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	N11	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	G8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	G7			
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	H8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	J8	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	L9	DQ3T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	M8			
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	B6	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	C7	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	E9	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	F8			
7B	VREFB7BN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	A7	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	A6	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	G9	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	H9			
7B	VREFB7BN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	D8	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS1T/CQ1T/CQn1T/QKn1T
7B	VREFB7BN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D9	DQSn4T/QK4T	DQ2T	DQSn1T/QK1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	A8	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B8			
7B	VREFB7BN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	A10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	B9	DQ4T	DQ2T	DQ1T

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7B	VREFB7BN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	J10	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	K10			
7C	VREFB7CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F10	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	G10	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	J11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	K11			
7C	VREFB7CN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	G11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	H11	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	K12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	L11			
7C	VREFB7CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	E11	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F11	DQSn5T/QK5T	DQSn3T/QK3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C10	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	D10			
7C	VREFB7CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	G12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	H12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L12	DQ5T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	M12			
7C	VREFB7CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	A11	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	B11	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO					N13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO	VREFB7CN0				M13			
7C	VREFB7CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	C11	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	D11	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	J13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	K13			
7C	VREFB7CN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	A13	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	B12	DQSn6T/QK6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	D12	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	E12			
7C	VREFB7CN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	F13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	G13	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	M11	DQ6T	DQ3T	DQ1T
7C	VREFB7CN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	N12			
7D	VREFB7DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	H14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	J14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	K14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	L14			
7D	VREFB7DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	F14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	G14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	M14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	M15			
7D	VREFB7DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	G15	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	H15	DQSn7T/QK7T	DQSn4T/QK4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	C13	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	D13			
7D	VREFB7DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	D14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	E14	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	K15	DQ7T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	L15			
7D	VREFB7DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	B14	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	C14	DQ8T	DQ4T	
7D	VREFB7DN0	IO					N15	DQ8T	DQ4T	
7D	VREFB7DN0	IO	VREFB7DN0				N14			
7D	VREFB7DN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	A14	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B15	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D15	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	E15			
7D	VREFB7DN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	F16	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	G16	DQSn8T/QK8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	J16	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	K16			
7D	VREFB7DN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	C16	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	D16	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	M16	DQ8T	DQ4T	
7D	VREFB7DN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	N16			
		VCCA_FPLL					R17			
		VCCD_FPLL					R16			
		DNU					L18			
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	A16	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	A17	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	K17	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	L17			
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	K18	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	K19	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	D17	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	E17			
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	F17	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T	

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	G17	DQSn9T/QK9T	DQSn5T/QK5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	M17	DQ9T	DQ5T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	N17			
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T67p	DIFFOUT_T67p	H17	DQ9T	DQ5T	
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T67n	DIFFOUT_T67n	J17	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	B17	DQ9T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	C17			
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T69p	DIFFOUT_T69p	A19	DQ10T	DQ5T	
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T69n	DIFFOUT_T69n	A20	DQ10T	DQ5T	
8D	VREFB8DN0	IO					M18	DQ10T	DQ5T	
8D	VREFB8DN0	IO	VREFB8DN0				N18			
8D	VREFB8DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	C19	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	B18	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T71p	DIFFOUT_T71p	G18	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T71n	DIFFOUT_T71n	G19			
8D	VREFB8DN0	IO			DIFFIO_RX_T72p	DIFFOUT_T72p	H18	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T72n	DIFFOUT_T72n	J19	DQSn10T/QK10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T73p	DIFFOUT_T73p	M19	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T73n	DIFFOUT_T73n	N19			
8D	VREFB8DN0	IO			DIFFIO_RX_T74p	DIFFOUT_T74p	D19	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_RX_T74n	DIFFOUT_T74n	D18	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T75p	DIFFOUT_T75p	E18	DQ10T	DQ5T	
8D	VREFB8DN0	IO			DIFFIO_TX_T75n	DIFFOUT_T75n	F19			
8C	VREFB8CN0	IO			DIFFIO_RX_T76p	DIFFOUT_T76p	K20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T76n	DIFFOUT_T76n	L20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO					M20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO	VREFB8CN0				N20			
8C	VREFB8CN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	A22	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	B21	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	B20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	C20			
8C	VREFB8CN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	D20	DQS11T/CQ11T/CQn11T/QKn11T	DQS6T/CQ6T/CQn6T/QKn6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	E20	DQSn11T/QK11T	DQSn6T/QK6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	K21	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	L21			
8C	VREFB8CN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	F20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	G20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	H20	DQ11T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	J20			
8C	VREFB8CN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	D21	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	E21	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	M21	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	N21			
8C	VREFB8CN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	C22	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	D22	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	G21	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	H21			
8C	VREFB8CN0	IO			DIFFIO_RX_T87p	DIFFOUT_T87p	F22	DQS12T/CQ12T/CQn12T/QKn12T	DQ6T	DQS2T/CQ2T/CQn2T/QKn2T
8C	VREFB8CN0	IO			DIFFIO_RX_T87n	DIFFOUT_T87n	G22	DQSn12T/QK12T	DQ6T	DQSn2T/QK2T
8C	VREFB8CN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	M22	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	N22			
8C	VREFB8CN0	IO			DIFFIO_RX_T89p	DIFFOUT_T89p	A23	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_RX_T89n	DIFFOUT_T89n	B23	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T90p	DIFFOUT_T90p	J22	DQ12T	DQ6T	DQ2T
8C	VREFB8CN0	IO			DIFFIO_TX_T90n	DIFFOUT_T90n	K22			
8B	VREFB8BN0	IO			DIFFIO_RX_T91p	DIFFOUT_T91p	H23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T91n	DIFFOUT_T91n	J23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	K24	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	L24			
8B	VREFB8BN0	IO			DIFFIO_RX_T93p	DIFFOUT_T93p	B24	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T93n	DIFFOUT_T93n	C23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T94p	DIFFOUT_T94p	D23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T94n	DIFFOUT_T94n	E23			
8B	VREFB8BN0	IO			DIFFIO_RX_T95p	DIFFOUT_T95p	F23	DQS13T/CQ13T/CQn13T/QKn13T	DQS7T/CQ7T/CQn7T/QKn7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T95n	DIFFOUT_T95n	G23	DQSn13T/QK13T	DQSn7T/QK7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T96p	DIFFOUT_T96p	M23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T96n	DIFFOUT_T96n	N23			
8B	VREFB8BN0	IO			DIFFIO_RX_T97p	DIFFOUT_T97p	D24	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T97n	DIFFOUT_T97n	E24	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T98p	DIFFOUT_T98p	K23	DQ13T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T98n	DIFFOUT_T98n	L23			
8B	VREFB8BN0	IO			DIFFIO_RX_T99p	DIFFOUT_T99p	G24	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T99n	DIFFOUT_T99n	H24	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO					M24	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO	VREFB8BN0				N24			
8B	VREFB8BN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	A26	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	A25	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	C25	DQ14T	DQ7T	DQ2T

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8B	VREFB8BN0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	D25			
8B	VREFB8BN0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	F25	DQS14T/CQ14T/CQn14T/QKn14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	G25	DQSn14T/QK14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	M25	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	N25			
8B	VREFB8BN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	B26	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	C26	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	J25	DQ14T	DQ7T	DQ2T
8B	VREFB8BN0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	K25			
8A	VREFB8AN0	IO			DIFFIO_RX_T106p	DIFFOUT_T106p	E26	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T106n	DIFFOUT_T106n	F26	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	K29	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	L29			
8A	VREFB8AN0	IO			DIFFIO_RX_T108p	DIFFOUT_T108p	D26	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T108n	DIFFOUT_T108n	E27	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T109p	DIFFOUT_T109p	A27	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T109n	DIFFOUT_T109n	B27			
8A	VREFB8AN0	IO			DIFFIO_RX_T110p	DIFFOUT_T110p	G26	DQS15T/CQ15T/CQn15T/QKn15T	DQS8T/CQ8T/CQn8T/QKn8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T110n	DIFFOUT_T110n	H26	DQSn15T/QK15T	DQSn8T/QK8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T111p	DIFFOUT_T111p	K27	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T111n	DIFFOUT_T111n	L27			
8A	VREFB8AN0	IO			DIFFIO_RX_T112p	DIFFOUT_T112p	D27	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T112n	DIFFOUT_T112n	C28	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T113p	DIFFOUT_T113p	C29	DQ15T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T113n	DIFFOUT_T113n	D28			
8A	VREFB8AN0	IO			DIFFIO_RX_T114p	DIFFOUT_T114p	G27	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T114n	DIFFOUT_T114n	G28	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	J26	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T115n	DIFFOUT_T115n	K26			
8A	VREFB8AN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	A29	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	A28	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T117p	DIFFOUT_T117p	B29	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T117n	DIFFOUT_T117n	B30			
8A	VREFB8AN0	IO			DIFFIO_RX_T118p	DIFFOUT_T118p	F28	DQS16T/CQ16T/CQn16T/QKn16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T118n	DIFFOUT_T118n	F29	DQSn16T/QK16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T119p	DIFFOUT_T119p	H27	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T119n	DIFFOUT_T119n	J27			
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T120p	DIFFOUT_T120p	D29	DQ16T	DQ8T	
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T120n	DIFFOUT_T120n	E29	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T121p	DIFFOUT_T121p	D30	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T121n	DIFFOUT_T121n	E30			
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T122p	DIFFOUT_T122p	G29	DQ17T		
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T122n	DIFFOUT_T122n	H29	DQ17T		
8A	VREFB8AN0	IO					L26	DQ17T		
8A	VREFB8AN0	IO	VREFB8AN0				M27			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T123p	DIFFOUT_T123p	A31	DQ17T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T123n	DIFFOUT_T123n	A30	DQ17T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T124p	DIFFOUT_T124p	C31	DQ17T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T124n	DIFFOUT_T124n	D31			
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T125p	DIFFOUT_T125p	A32	DQS17T/CQ17T/CQn17T/QKn17T		
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T125n	DIFFOUT_T125n	B32	DQSn17T/QK17T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	J28	DQ17T		
8A	VREFB8AN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	K28			
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T127p	DIFFOUT_T127p	D33	DQ17T		
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T127n	DIFFOUT_T127n	C32	DQ17T		
8A	VREFB8AN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	D32	DQ17T		
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T128n	DIFFOUT_T128n	E32			
8A		MSEL0		MSEL0			D34			
8A		MSEL1		MSEL1			H30			
8A		MSEL2		MSEL2			K30			
8A		MSEL3		MSEL3			M29			
8A		MSEL4		MSEL4			M30			
8A		CONF_DONE		CONF_DONE			C34			
8A		nSTATUS		nSTATUS			B34			
8A		nCE		nCE			A33			
8A		nCONFIG		nCONFIG			C33			
		GND					B33			
		GND					AA26			
		GND					AA33			
		GND					AA34			
		GND					AB27			
		GND					AB28			
		GND					AB29			
		GND					AB30			
		GND					AB31			
		GND					AB32			
		GND					AC30			
		GND					AC33			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AC34			
		GND					AD31			
		GND					AD32			
		GND					AE30			
		GND					AE33			
		GND					AE34			
		GND					AF31			
		GND					AF32			
		GND					AG30			
		GND					AG33			
		GND					AG34			
		GND					AH31			
		GND					AH32			
		GND					AJ30			
		GND					AJ33			
		GND					AJ34			
		GND					AK31			
		GND					AK32			
		GND					AL33			
		GND					AL34			
		GND					E34			
		GND					F31			
		GND					F32			
		GND					G30			
		GND					G33			
		GND					G34			
		GND					H31			
		GND					H32			
		GND					J30			
		GND					J33			
		GND					J34			
		GND					K31			
		GND					K32			
		GND					L30			
		GND					L33			
		GND					L34			
		GND					M31			
		GND					M32			
		GND					N28			
		GND					N29			
		GND					N33			
		GND					N34			
		GND					P27			
		GND					P31			
		GND					P32			
		GND					R28			
		GND					R30			
		GND					R33			
		GND					R34			
		GND					T27			
		GND					T29			
		GND					T31			
		GND					T32			
		GND					U28			
		GND					U33			
		GND					U34			
		GND					V27			
		GND					V31			
		GND					V32			
		GND					W28			
		GND					W30			
		GND					W33			
		GND					W34			
		GND					Y27			
		GND					Y29			
		GND					Y31			
		GND					Y32			
		GND					AA1			
		GND					AA2			
		GND					AA9			
		GND					AB3			
		GND					AB4			
		GND					AB5			
		GND					AB7			
		GND					AB8			
		GND					AC1			
		GND					AC2			
		GND					AC5			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AD3			
		GND					AD4			
		GND					AE1			
		GND					AE2			
		GND					AE5			
		GND					AF3			
		GND					AF4			
		GND					AG1			
		GND					AG2			
		GND					AG5			
		GND					AH3			
		GND					AH4			
		GND					AJ1			
		GND					AJ2			
		GND					AJ5			
		GND					AK3			
		GND					AK4			
		GND					AL1			
		GND					AL2			
		GND					AL3			
		GND					AN1			
		GND					F3			
		GND					F4			
		GND					G1			
		GND					G2			
		GND					G5			
		GND					H3			
		GND					H4			
		GND					J1			
		GND					J2			
		GND					J5			
		GND					K3			
		GND					K4			
		GND					L1			
		GND					L2			
		GND					L5			
		GND					M3			
		GND					M4			
		GND					M5			
		GND					N1			
		GND					N2			
		GND					N6			
		GND					P3			
		GND					P4			
		GND					P8			
		GND					R1			
		GND					R2			
		GND					R5			
		GND					R7			
		GND					T3			
		GND					T4			
		GND					T6			
		GND					T8			
		GND					U1			
		GND					U2			
		GND					U7			
		GND					V3			
		GND					V4			
		GND					V8			
		GND					W1			
		GND					W2			
		GND					W5			
		GND					W7			
		GND					Y3			
		GND					Y4			
		GND					Y6			
		GND					Y8			
		VCCP					P18			
		VCCP					R13			
		VCCP					R21			
		VCCP					T10			
		VCCP					U25			
		VCCP					V10			
		VCCP					W25			
		VCCP					Y12			
		VCCP					Y19			
		VCCP					Y22			
		VCCA_FPLL					V26			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCA_FPLL					V9			
		VCCA_FPLL					T26			
		VCCA_FPLL					T9			
		VCCBAT					M28			
		VCC_AUX					P12			
		VCC_AUX					P24			
		VCC_AUX					W11			
		VCC_AUX					Y24			
		VCCD_FPLL					Y26			
		VCCD_FPLL					Y9			
		VCCD_FPLL					P26			
		VCCD_FPLL					P9			
		VCCA_GXBL0					Y28			
		VCCA_GXBR0					Y7			
		VCCA_GXBL1					T28			
		VCCA_GXBR1					T7			
		VCCH_GXBL0					V28			
		VCCH_GXBR0					V7			
		VCCH_GXBL1					P28			
		VCCH_GXBR1					P7			
		VCCL_GXBL0					V29			
		VCCL_GXBL0					V30			
		VCCL_GXBR0					V5			
		VCCL_GXBR0					V6			
		VCCL_GXBL1					P29			
		VCCL_GXBL1					P30			
		VCCL_GXBR1					P5			
		VCCL_GXBR1					P6			
		VCCR_GXBL					AA29			
		VCCR_GXBL					AA30			
		VCCR_GXBL					N30			
		VCCR_GXBL					U29			
		VCCR_GXBL					U30			
		VCCR_GXBR					AA5			
		VCCR_GXBR					AA6			
		VCCR_GXBR					N5			
		VCCR_GXBR					U5			
		VCCR_GXBR					U6			
		VCCT_GXBL0					W29			
		VCCT_GXBL0					Y30			
		VCCT_GXBR0					W6			
		VCCT_GXBR0					Y5			
		VCCT_GXBL1					R29			
		VCCT_GXBL1					T30			
		VCCT_GXBR1					R6			
		VCCT_GXBR1					T5			
		VCC					R14			
		VCC					R15			
		VCC					R19			
		VCC					R23			
		VCC					R25			
		VCC					T12			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					T20			
		VCC					T22			
		VCC					T24			
		VCC					U11			
		VCC					U12			
		VCC					U13			
		VCC					U15			
		VCC					U17			
		VCC					U19			
		VCC					U20			
		VCC					U21			
		VCC					U22			
		VCC					U23			
		VCC					V12			
		VCC					V14			
		VCC					V16			
		VCC					V20			
		VCC					V22			
		VCC					V24			
		VCC					W13			
		VCC					W15			
		VCC					W17			
		VCC					W19			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCC					W21			
		VCC					W23			
		VCC					Y13			
		VCC					Y20			
		VCC					V18			
		VCCIO3A					AD30			
		VCCIO3A					AF27			
		VCCIO3A					AH30			
		VCCIO3A					AJ27			
		VCCIO3A					AK30			
		VCCIO3A					AM27			
		VCCIO3B					AF24			
		VCCIO3B					AJ24			
		VCCIO3B					AM24			
		VCCIO3B					AP24			
		VCCIO3C					AF21			
		VCCIO3C					AJ21			
		VCCIO3C					AM21			
		VCCIO3C					AP21			
		VCCIO3D					AF18			
		VCCIO3D					AJ18			
		VCCIO3D					AM18			
		VCCIO3D					AP18			
		VCCIO4A					AD5			
		VCCIO4A					AF5			
		VCCIO4A					AH5			
		VCCIO4A					AK5			
		VCCIO4B					AF9			
		VCCIO4B					AJ9			
		VCCIO4B					AM9			
		VCCIO4B					AP9			
		VCCIO4C					AF12			
		VCCIO4C					AJ12			
		VCCIO4C					AM12			
		VCCIO4C					AP12			
		VCCIO4D					AF15			
		VCCIO4D					AJ15			
		VCCIO4D					AM15			
		VCCIO4D					AP15			
		VCCIO7A					C5			
		VCCIO7A					F2			
		VCCIO7A					F5			
		VCCIO7A					L7			
		VCCIO7B					A9			
		VCCIO7B					C9			
		VCCIO7B					F9			
		VCCIO7B					J9			
		VCCIO7C					A12			
		VCCIO7C					C12			
		VCCIO7C					F12			
		VCCIO7C					J12			
		VCCIO7D					A15			
		VCCIO7D					C15			
		VCCIO7D					F15			
		VCCIO7D					J15			
		VCCIO8A					C27			
		VCCIO8A					C30			
		VCCIO8A					F27			
		VCCIO8A					F30			
		VCCIO8A					J29			
		VCCIO8A					M26			
		VCCIO8B					A24			
		VCCIO8B					C24			
		VCCIO8B					F24			
		VCCIO8B					J24			
		VCCIO8C					A21			
		VCCIO8C					C21			
		VCCIO8C					F21			
		VCCIO8C					J21			
		VCCIO8D					A18			
		VCCIO8D					C18			
		VCCIO8D					F18			
		VCCIO8D					J18			
		VCCPD3					AB26			
		VCCPD3					AC27			
		VCCPD3					Y21			
		VCCPD3					Y25			
		VCCPD4A					AB6			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCPD4A					AB9			
		VCCPD4BCD					Y10			
		VCCPD4BCD					Y14			
		VCCPD4BCD					Y16			
		VCCPD7A					N8			
		VCCPD7A					N9			
		VCCPD7BCD					P14			
		VCCPD7BCD					P16			
		VCCPD7BCD					R11			
		VCCPD8					N26			
		VCCPD8					N27			
		VCCPD8					P20			
		VCCPD8					P22			
		VCCPGM					M9			
		VCCPGM					AC26			
		GND					AA11			
		GND					AA13			
		GND					AA16			
		GND					AA19			
		GND					AA22			
		GND					AA24			
		GND					AD10			
		GND					AD13			
		GND					AD16			
		GND					AD19			
		GND					AD22			
		GND					AD25			
		GND					AD28			
		GND					AD7			
		GND					AG10			
		GND					AG13			
		GND					AG16			
		GND					AG19			
		GND					AG22			
		GND					AG25			
		GND					AG28			
		GND					AG7			
		GND					AK10			
		GND					AK13			
		GND					AK16			
		GND					AK19			
		GND					AK22			
		GND					AK25			
		GND					AK28			
		GND					AK7			
		GND					AN10			
		GND					AN13			
		GND					AN16			
		GND					AN19			
		GND					AN22			
		GND					AN25			
		GND					AN28			
		GND					AN31			
		GND					AN4			
		GND					AN7			
		GND					B1			
		GND					B10			
		GND					B13			
		GND					B16			
		GND					B19			
		GND					B22			
		GND					B25			
		GND					B28			
		GND					B31			
		GND					B4			
		GND					B7			
		GND					D2			
		GND					D4			
		GND					E10			
		GND					E13			
		GND					E16			
		GND					E19			
		GND					E22			
		GND					E25			
		GND					E28			
		GND					E31			
		GND					E7			
		GND					H10			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					H13			
		GND					H16			
		GND					H19			
		GND					H22			
		GND					H25			
		GND					H28			
		GND					H7			
		GND					L10			
		GND					L13			
		GND					L16			
		GND					L19			
		GND					L22			
		GND					L25			
		GND					L28			
		GND					L8			
		GND					M6			
		GND					N7			
		GND					P10			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P19			
		GND					P21			
		GND					P23			
		GND					P25			
		GND					R10			
		GND					R12			
		GND					R18			
		GND					R20			
		GND					R22			
		GND					R24			
		GND					T11			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					T23			
		GND					T25			
		GND					U10			
		GND					U14			
		GND					U16			
		GND					U24			
		GND					V11			
		GND					V13			
		GND					V15			
		GND					V17			
		GND					V19			
		GND					V21			
		GND					V23			
		GND					V25			
		GND					W10			
		GND					W12			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W20			
		GND					W22			
		GND					W24			
		GND					U18			

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	11/4/2011	Preliminary release.
1.1	1/3/2012	Split VCC to VCC and VCCP
1.2	1/23/2013	- Removed Preliminary - Rename the CQ and DQS pins in DQS and hard memory PHY columns