Sub-Bank	Package Name	Index within I/O Bank (Bottom Sub-Bank Index/Top Sub-Bank Index)	Index within I/O Lane	DDR4 Scheme 1: Component and DIMM (Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	DDR4 Scheme 1A: Component, LRDIMM and RDIMM (with base component x16Gb x4DQ/DQS group)	DDR4 Scheme 2: Component and DIMM (Supports up to 2 ranks for UDIMM/RDIMM/SO-DIMM/Component) *ONLY scheme for HPS EMIF* Available to Fabric EMIF as well	DDR4 Scheme 3: Component and DIMM, with 3DS (Support 3DS; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	DDR4 Scheme 3A: Component and DIMM, with 3DS (Support 3DS; Supports up to 4 ranks for UDIMM/RDIMM/SO-DIMM/Component)	QDR-IV Scheme 1
Lane 3	LVDSXX_1N	47 / 95	11	CK_N_1	CK_N_1	Not used by Address/Command pins in this scheme; usable as Data pins. In HPS mode, ECC pins must be placed here.	CK_N_1	CK_N_1	LBK1_N_0
	LVDSXX_1P	46 / 94	10	CK_1	CK_1		CK_1	CK_1	LBK0_N_0
	LVDSXX_2N	45 / 93	9	CK_N_3					A_24
	LVDSXX_2P	44 / 92	8	CK_3	ALERT_N			ALERT_N	A_23
	LVDSXX_3N	43 / 91	7	CK_N_2			CS_3	CS_3	
	LVDSXX_3P	42 / 90	6	CK_2			CS_2	CS_2	AP
	LVDSXX_4N	41 / 89	5	CKE_3			CKE_3	CKE_3	
	LVDSXX_4P	40 / 88	4	CKE_2			CKE_2	CKE_2	
	LVDSXX_5N	39 / 87	3	ODT_3			ODT_3	ODT_3	A_22
	LVDSXX_5P	38 / 86	2	ODT_2			ODT_2	ODT_2	A_21
	LVDSXX_6N	37 / 85	1	CS_N_3			C_1	C_1	A_20
	LVDSXX_6P	36 / 84	0	CS_N_2			C_0	C_0	A_19
Lane 2	LVDSXX_7N	35 / 83	11	BG_0	BG_0	BG_0	BG_0	BG_0	A_18
	LVDSXX_7P	34 / 82	10	BA_1	BA_1	BA_1	BA_1	BA_1	A_17
	LVDSXX_8N	33 / 81	9	BA_0	BA_0	BA_0	BA_0	BA_0	A_16
	LVDSXX_8P	32 / 80	8	ALERT_N	A_17	ALERT_N	ALERT_N	A_17	A_15
	LVDSXX_9N	31 / 79	7	A_16	A_16	A_16	A_16	A_16	PE_N
	LVDSXX_9P	30 / 78	6	A_15	A_15	A_15	A_15	A_15	A_14
	LVDSXX_10N	29 / 77	5	A_14	A_14	A_14	A_14	A_14	
	LVDSXX_10P	28 / 76	4	A_13	A_13	A_13	A_13	A_13	
	LVDSXX_11N	27 / 75	3	A_12	A_12	A_12	A_12	A_12	A_13
	LVDSXX_11P	26 / 74	2	RZQ Site□					
	LVDSXX_12N	25 / 73	1	Differential "N-Side" Reference Clock Input Site (LVDS Reference Clock Only)□					
	LVDSXX_12P	24 / 72	0	Single-Ended or Differential "P-Side" PLL Reference Clock Input Site□					
Lane 1	LVDSXX_13N	23 / 71	11	A_11	A_11	A_11	A_11	A_11	A_12
	LVDSXX_13P	22 / 70	10	A_10	A_10	A_10	A_10	A_10	A_11
	LVDSXX_14N	21 / 69	9	A_9	A_9	A_9	A_9	A_9	A_10
	LVDSXX_14P	20 / 68	8	A_8	A_8	A_8	A_8	A_8	A_9
	LVDSXX_15N	19 / 67	7	A_7	A_7	A_7	A_7	A_7	RESET_N_0
	LVDSXX_15P	18 / 66	6	A_6	A_6	A_6	A_6	A_6	A_8
	LVDSXX_16N	17 / 65	5	A_5	A_5	A_5	A_5	A_5	
	LVDSXX_16P	16 / 64	4	A_4	A_4	A_4	A_4	A_4	
	LVDSXX_17N	15 / 63	3	A_3	A_3	A_3	A_3	A_3	A_7
	LVDSXX_17P	14 / 62	2	A_2	A_2	A_2	A_2	A_2	A_6
	LVDSXX_18N	13 / 61	1	A_1	A_1	A_1	A_1	A_1	A_5
	LVDSXX_18P	12 / 60	0	A_0	A_0	A_0	A_0	A_0	A_4
Lane 0	LVDSXX_19N	11 / 59	11	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	A_3
	LVDSXX_19P	10 / 58	10	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1	A_2
	LVDSXX_20N	9 / 57	9	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	A_1
	LVDSXX_20P	8 / 56	8	CK_0	CK_0	CK_0	CK_0	CK_0	A_0
	LVDSXX_21N	7 / 55	7	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	CFG_N_0
	LVDSXX_21P	6 / 54	6	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	AINV_0
	LVDSXX_22N	5 / 53	5	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	CK_N_0
	LVDSXX_22P	4 / 52	4	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	CK_0
	LVDSXX_23N	3 / 51	3	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	LDB_N_0
	LVDSXX_23P	2 / 50	2	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	LDA_N_0
	LVDSXX_24N	1 / 49	1	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RWB_N_0
	LVDSXX_24P	0 / 48	0	BG_1	BG_1	BG_1	BG_1	BG_1	RWA_N_0

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Date	Version	Changes Made
July 2019	2019.07.17	Initial release.
February 2020	2020.02.18	Updated the header column title from "Index Within I/O Sub-bank" to "Index Within I/O Lane".
April 2020	2020.04.30	- Added the top/bottom sub-bank index in column C. - Updated the header column title of column G, available in EMIF fabric as well. - Removed the RLDRAM3 column (not supported).
October 2021	2021.10.04	- Updated document status to final. - Updated the header column title from "Index within I/O Bank (Top Sub-Bank Index/Bottom Sub-Bank Index)" to "Index within I/O Bank (Bottom Sub-Bank Index/Top Sub-Bank Index)".

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