Implementing QPI Using the Transceiver Native PHY IP Core in Stratix V Devices

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This application note describes how to implement the Intel® QuickPath Interconnect (QPI) protocol with Altera® transceivers in the Stratix® V devices. Designers can create the QPI interface design using FPGA logic to interface with the transceiver configurations described in this document.

Stratix V Native PHY IP cores provide an easy and efficient method to implement the QPI protocol.

QPI Overview

The QPI is a point-to-point connection protocol developed by Intel to replace the front-side-bus (FSB). It was designed to transfer data between the processors and IO hubs. Compared to a parallel bus, the QPI can achieve higher performance.

QPI is a serial bus technology similar to other point-to-point interconnects. All channels work at the differential IO standard. The physical data rates for QPI can be 4.8, 6.4, or 8 Gbps. The channel links can be defined as full-width for 20 channels, and half-width for 10 channels.

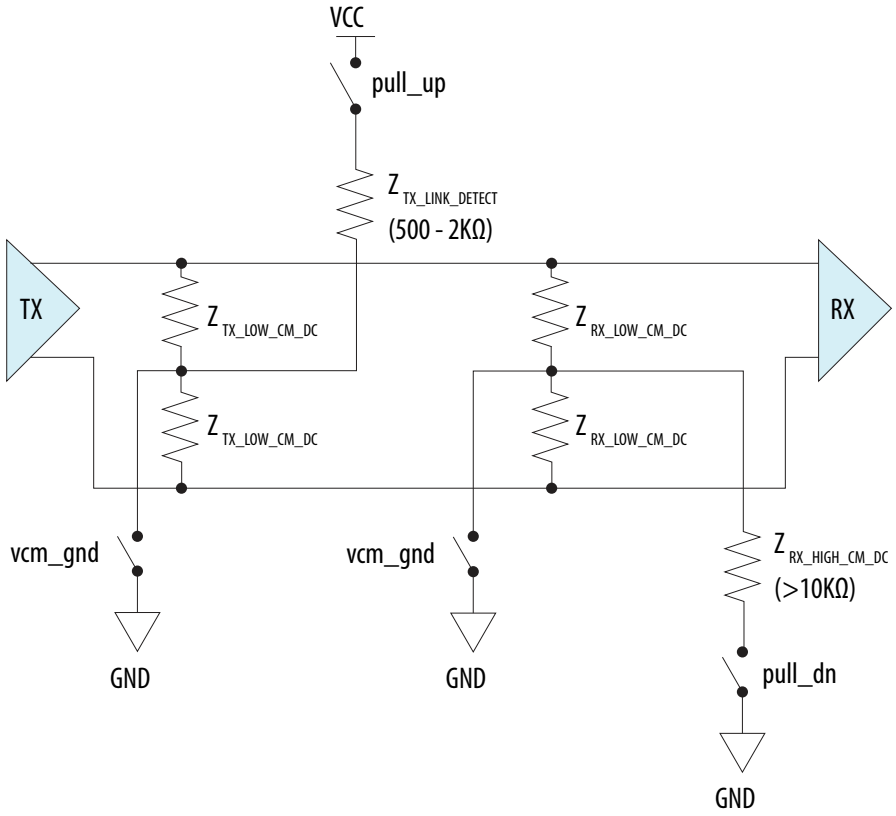
QPI has the following special features, which may differ from other serial interface protocols:

- **DC Coupling Mode**

The transmitter (TX) and receiver (RX) use DC coupling mode. Per the QPI spec, the connected transceiver pair are DC-coupled.

Stratix V devices have been characterized to be fully compatible with DC mode for QPI interfaces. From the transmitter, the output common mode DC voltage can vary between 0.23 to 0.27 V.

Figure 1: DC Mode



Notes :

(1) $Z_{TX\_LOW\_CM\_DC} = Z_{RX\_LOW\_CM\_DC} = 85\Omega$. It is turned **On** in the steady-state mode with $Z_{TX\_LINK\_DETECT}$ and $Z_{RX\_HIGH\_CM\_DC}$ **Off**.

(2) $Z_{RX\_HIGH\_CM\_DC}$ are pull down resistors (> 10KΩ), which are turned **Off** in the steady-state mode.

(3) Both $Z_{TX\_LOW\_CM\_DC}$ and $Z_{RX\_LOW\_CM\_DC}$ are implemented on all TX, RX, and clock pins .

(4) $Z_{TX\_LINK\_DETECT}$ are weak pull up resistors (500 ~ 2KΩ), and only implemented in TX pins. They are used in the Init phase and are **Off** in the steady-state mode.

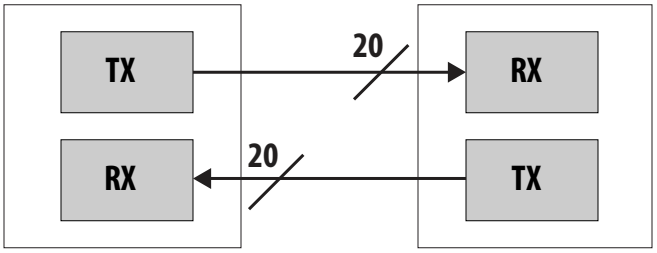
- **Bonded TX Channels**

All the TX channels must be configured in bonded mode to reduce the channel-to-channel skew. For example, full-width link design will bond all 20 TX channels together.

Stratix V devices can support TX channel bonding for QPI with PLL feedback compensation mode.

To bond all channels using the PLL feedback compensation path, the input reference clock frequency used by the TX PLL must be the same as the parallel clock that clocks the PCS of the same channel. For example, the reference clock is 250 MHz for an 8 Gbps data rate and 200 MHz for 6.4 Gbps.

Figure 2: Bonded Channels



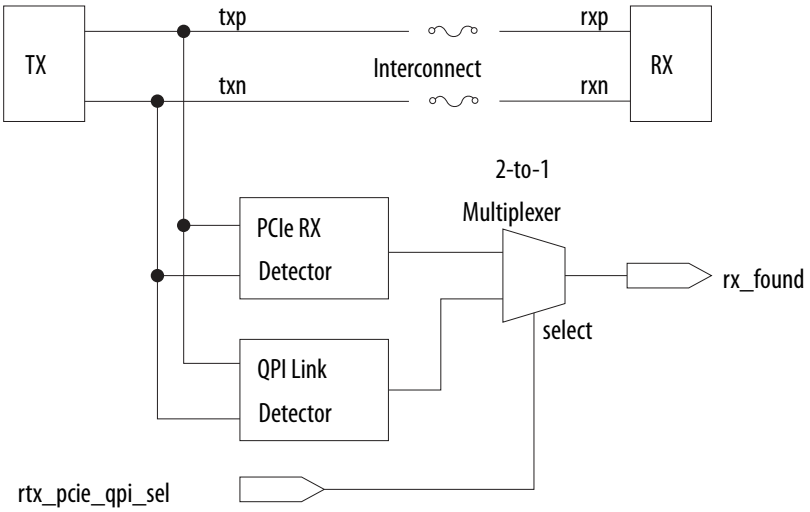
- **QPI Link Detection**

The Intel QPI physical layer uses a TX based detect scheme. Each TX lane contains a link detect circuit on each TXP and TXN.

During QPI link detecting, the transmitter driver will be tri-stated to avoid interference.

Stratix V devices support the PCIe RX detector and QPI link detector in the transmitter buffer. An assignment setting is used to select QPI mode or PCIe mode. When enabling QPI link detection, the QPI link detector will assert `rx_found` if a remote RX exists with a 42.5Ω termination.

Figure 3: Link Detection



Using the Native PHY IP Core for QPI

Use the Native PHY IP core to implement QPI for a low latency requirement.

The Native PHY IP core provides direct access to the PMA from the FPGA fabric in PMA Direct mode. Consequently, the latency for transmitted and received data is very low.

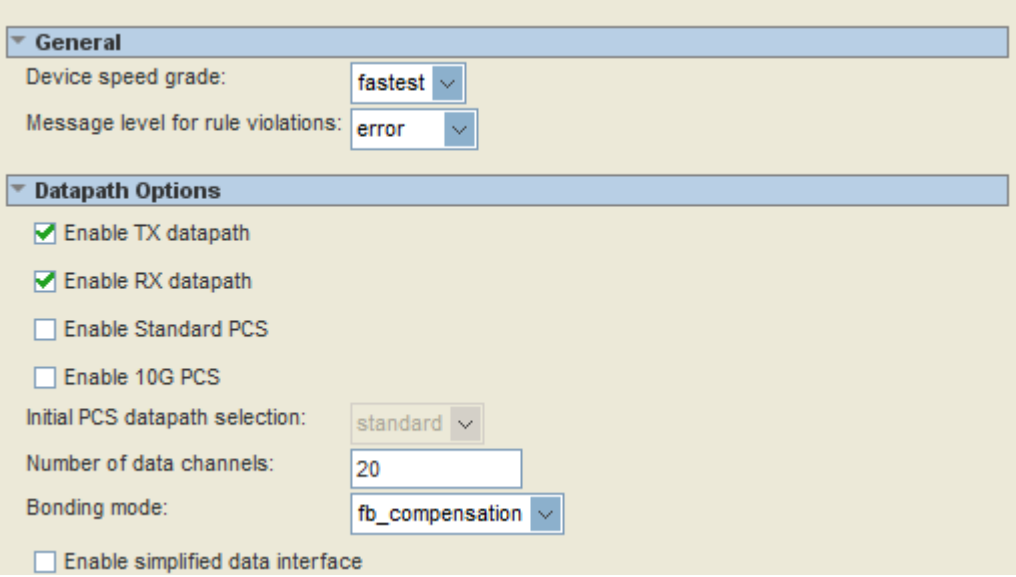
Use the following steps to implement QPI with the necessary options and settings, using the Native PHY IP core:

1. Configure the Native PHY IP core

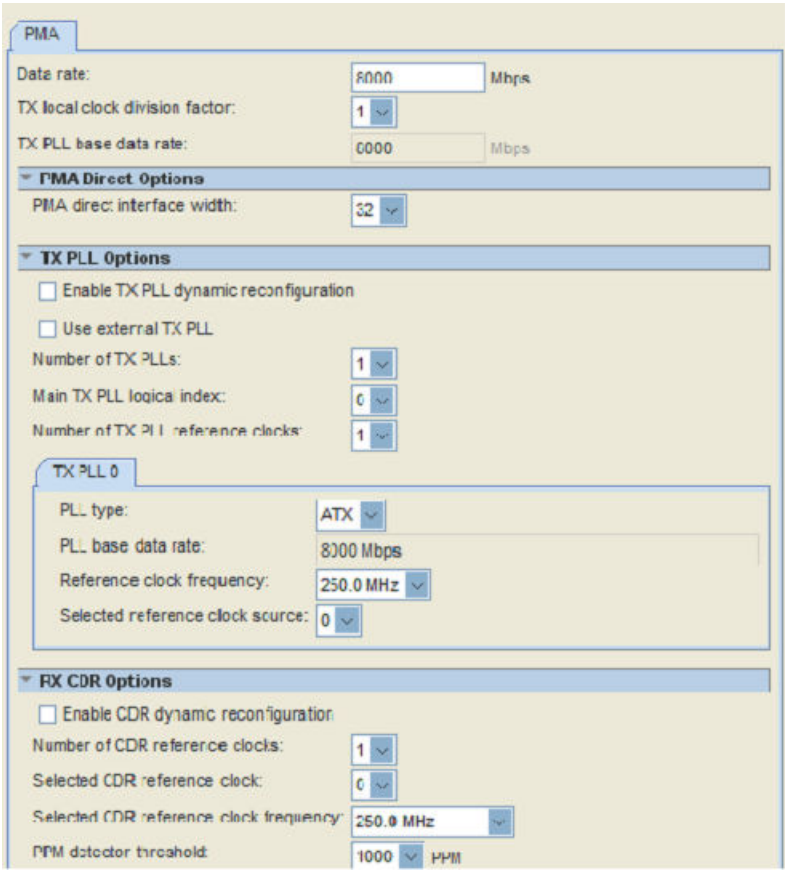
After the Stratix V Transceiver Native PHY IP core opens in the MegaWizard™ Plug-In Manager, the **General** tab and block diagram appear. The **General** tab contains the general settings for the Native PHY IP core.

For example, design an 8 Gbps QPI as a full-width link using the **Datapath Options**.

a. Select **Enable TX datapath** and **Enable RX datapath**.
b. Set the **Number of data channels** to **20**.
c. Set the **Bonding mode** to **fb_compensation**.



d. In the **PMA** tab, input the **Data rate** as **8000 Mbps**.
e. In **PMA Direct Options**, set the **PMA direct interface width** to **32**.
f. In the **TX PLL 0** tab, select the **PLL type** as **ATX**, and set the **Reference clock frequency** to **250.0 MHz**.
g. In **RX CDR Options**, set the **Selected CDR reference clock frequency** to **250.0 MHz**.



h. In **PMA Optional Ports**, enable the ports for the QPI features:

- **tx_pma_qpipullup**
- **tx_pma_qpipulldn**
- **tx_pma_txdetectrx**
- **tx_pma_rxfound**
- **rx_pma_qpipulldn**

i. Click **Finish** in the MegaWizard Plug-In Manager.

2. Enable the QPI Setting for the Transceiver

   Open the <*project_name*>**.qsf** file and input the following settings.

   Termination

- `set_instance_assignment -name XCVR_IO_PIN_TERMINATION 85_OHMS -to tx_serial_data[0]`
- `set_instance_assignment -name XCVR_IO_PIN_TERMINATION 85_OHMS -to rx_serial_data[0]`

QPI Enable

- `set_instance_assignment -name XCVR_RX_QPI_ENABLE ON -to rx_serial_data`
- `set_instance_assignment -name XCVR_TX_QPI_EN ON -to tx_serial_data`

DC Coupling Support

- `set_instance_assignment -name XCVR_TX_VCM_CTRL_SRC DYNAMIC_CTL -to tx_serial_data[0]`
- `set_instance_assignment -name XCVR_RX_INPUT_VCM_SEL LOW_VCM -to rx_serial_data[0]`

Link Detection

- `set_instance_assignment -name XCVR_TX_RX_DET_OUTPUT_SEL RX_DET_QPI_OUT -to tx_serial_data[0]`

Note: For more information about QSF settings, refer to the *Quartus Settings File Reference Manual*.

3. Link the Detection Design Flow

   To enable RX link detection at the transmitter side, the transmitter driver must be set as tri-state. During the normal data transferring state, the transmitter driver must be enabled.

   The `rtx_pdb` bit is used to control the transmitter buffer in tri-state. It can be accessed through the Streamer mode 3 in the transceiver reconfiguration controller.

1	Register	Field Name	Field Bit Offset	Field Bit Width	Field Access
28	ch_reg_2	rtx_pdb	15	1	rw

   Bit[15] of `rtx_pdb` must be set to **0** before the link detection function is triggered. Writing a **1** to the `rtx_pdb` bit will set the transmitter buffer in normal mode. The other bits at this address cannot be modified.

Related Information

Quartus Settings File Reference Manual

Setting the Transmitter Driver to Tri-State

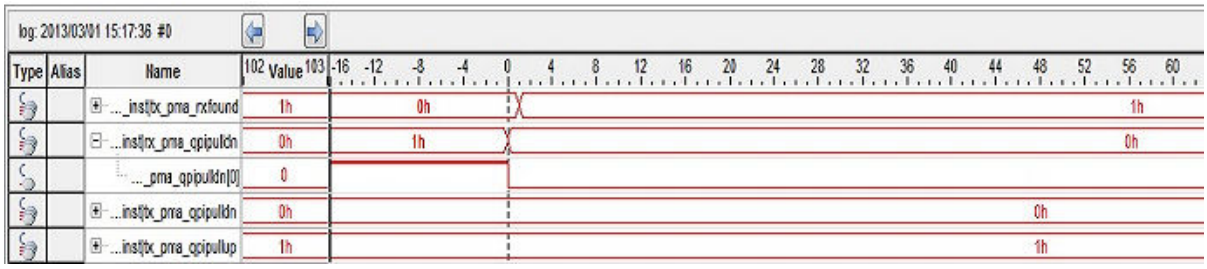
Use the procedure below to set the transmitter driver to tri-state using Streamer mode 3.

To set the transmitter driver to tri-state:

1. Ensure that the transceiver reconfiguration controller is correctly connected to the Native PHY IP core.
2. Enable the **.MIF** streamer module by selecting the **Enable channel/PLL reconfiguration** option in the transceiver reconfiguration controller.
3. Write the logical channel number to address **0x38**.
4. Write the MIF mode **0xC** to address **0x3A**.
5. Write the `rtx_pdb` address **0x25A** to address **0x3B**.
6. Write the Control and status register with a value of **0xE** to address **0x3A** to initiate a read.
7. Read address **0x3c**.

8. With the data obtained from step 7, perform a RMW with the 15-bit data pattern that selects the `rtx_pdb` bit.
9. Write the data pattern generated from step **8** to address **0x3C**.
10. Write the Control and status register with a value of **0xD** to address **0x3A**.

After changing `rtx_pdb` to **0** to set the transmitter driver in tri-state, `tx_pma_rxfound` will go high after asserting `tx_pma_txdetectrx` and `tx_pma_qpipullup`, if the RX link exists with a 42.5Ω termination, as shown in the following figure.



Related Information

For more information, refer to the "Transceiver Reconfiguration Controller IP Core Section" in the Altera Transceiver PHY IP Core User Guide.

Document Revision History

Table 1: Document Revision History

Date	Version	Change
December 2015	2015.12.17	Added a link to the *Quartus Settings File Reference Manual* in the "Using the Native PHY IP Core for QPI" section.
May 2013	2013.05.29	Initial release.