Serial Digital Interface Reference Design for Stratix V GX and Arria V GX Devices

Introduction

The Serial Digital Interface (SDI) reference design shows how you can transmit and receive video data using the Altera® SDI MegaCore® function, with the Stratix® V GX FPGA development kit or the Arria® V GX starter kit. This reference design uses two instances of the SDI MegaCore function. The triple standard SDI MegaCore function comprises of a standard definition (SD-SDI), a high definition (HD-SDI), and a 3 gigabits per second (3G-SDI) standard.

This application note describes how to use the serial digital interface with the Stratix V GX FPGA development kit and the Arria V GX starter kit for different variants.

For more information about the Stratix V GX FPGA development kit, refer to the *Stratix V GX FPGA Development Board Reference Manual*. For more information about the Arria V GX starter kit, refer to the *Arria V GX Starter Board Reference Manual*. For more information about the SDI HSMC, refer to the *SDI HSMC Reference Manual*. For more information about the SDI MegaCore function, refer to the *SDI MegaCore Function User Guide* or contact your Altera representative.

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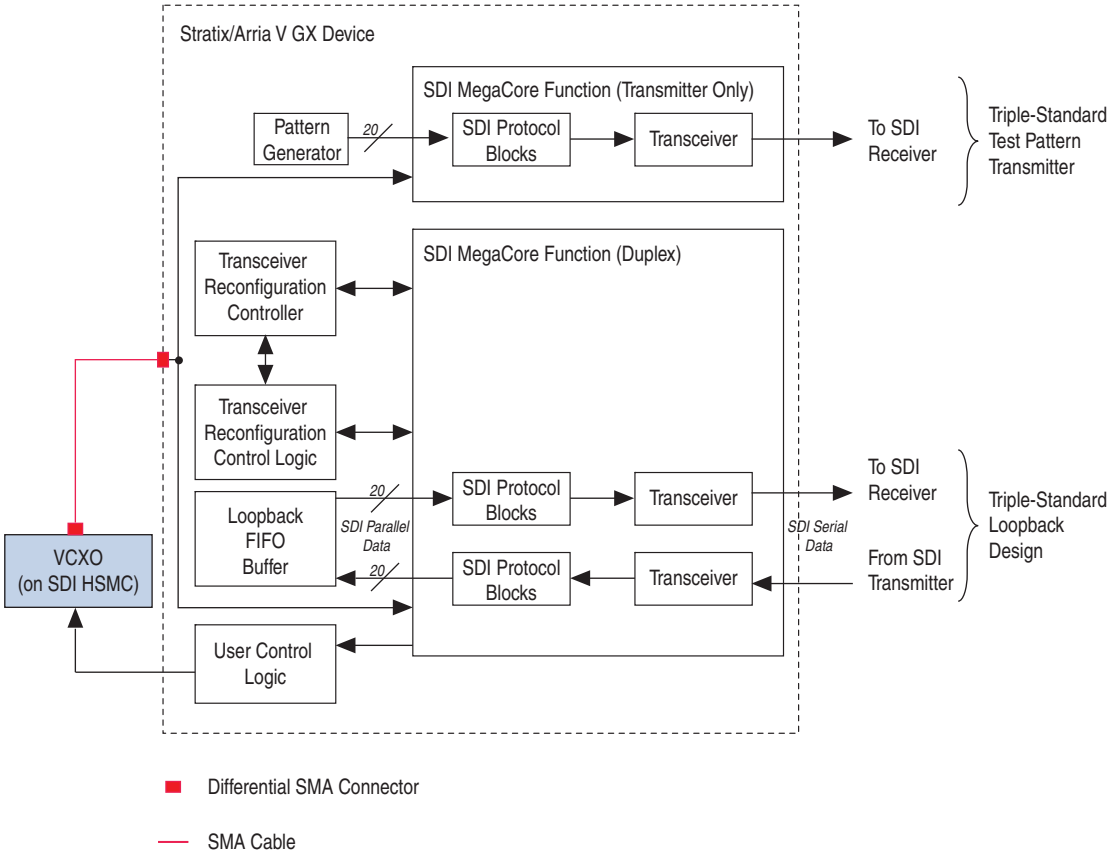
Functional Description

The reference design provides a general platform to control, test, and monitor different speeds of the SDI operations. Figure 1 shows a high-level block diagram of the SDI reference design.

Figure 1. Block Diagram



The following sections describe the various elements in Figure 1.

Triple-Standard Transmitter

The triple-standard SDI transmitter MegaCore function outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i, or 270-Mbps data stream. The transmitter takes its input from the pattern generator.

Triple-Standard Loopback

The triple-standard SDI MegaCore function provides HD-SDI, and SD-SDI, and demonstrates receiver-to-transmitter loopback. The transceiver decodes, buffers, recodes, and transmits the received data.

The interface supports 2.970-Gbps, 1.485-Gbps, or 270-Mbps loopback FIFO buffer. The FIFO buffer connects the decoded receiver data to the transmitter input.

The SDI MegaCore function writes the receiver data to the FIFO buffer when the receiver is in the lock position. When the FIFO buffer is half full, the transmitter starts to read, encode, and transmit the data.

Pattern Generator

The pattern generator IP core outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i or 270-Mbps test pattern. This test pattern can be a 100% color bar, a 75% amplitude color bar, or an SDI pathological checkfield frame.

Transceiver Reconfiguration Control Logic

The transceiver reconfiguration control logic reconfigures the receiver part of the design's duplex core, and the separate receiver in the design. The reconfiguration control logic contains a state machine to change the transceiver setting using MIF-based reconfiguration method.

For more information about the transceivers, refer to the Transceiver Reconfiguration Controller section in the *Altera Transceiver PHY IP Core User Guide*.

Transceiver Reconfiguration Controller

The dynamic partial reconfigurable I/O (DPRIO) requires the transceiver reconfiguration controller IP instance block. You can also use this block to reprogram the custom PHY transceivers.

Clock Input Differential SMA Connectors

The 148.5-MHz clock source from the HSMC feeds to `rx_serial_refclk` and `tx_serial_refclk` signals through external SMA cables because of hardware limitation in the development board. The SMA cables connect the SDI clock output from the HSMC to the clock input differential. Apply an external clock source from the clock input differential SMA connectors to the receiver instance in this design.

Altera recommends you to use the dedicated clock pin to feed the reference clock.

User Control Logic

The user control logic receives the CDR receiver clock, `rx_clk`, from the SDI receiver only and the SDI duplex instances, and then sends the receiver clock with the control bits to the VCXO device.

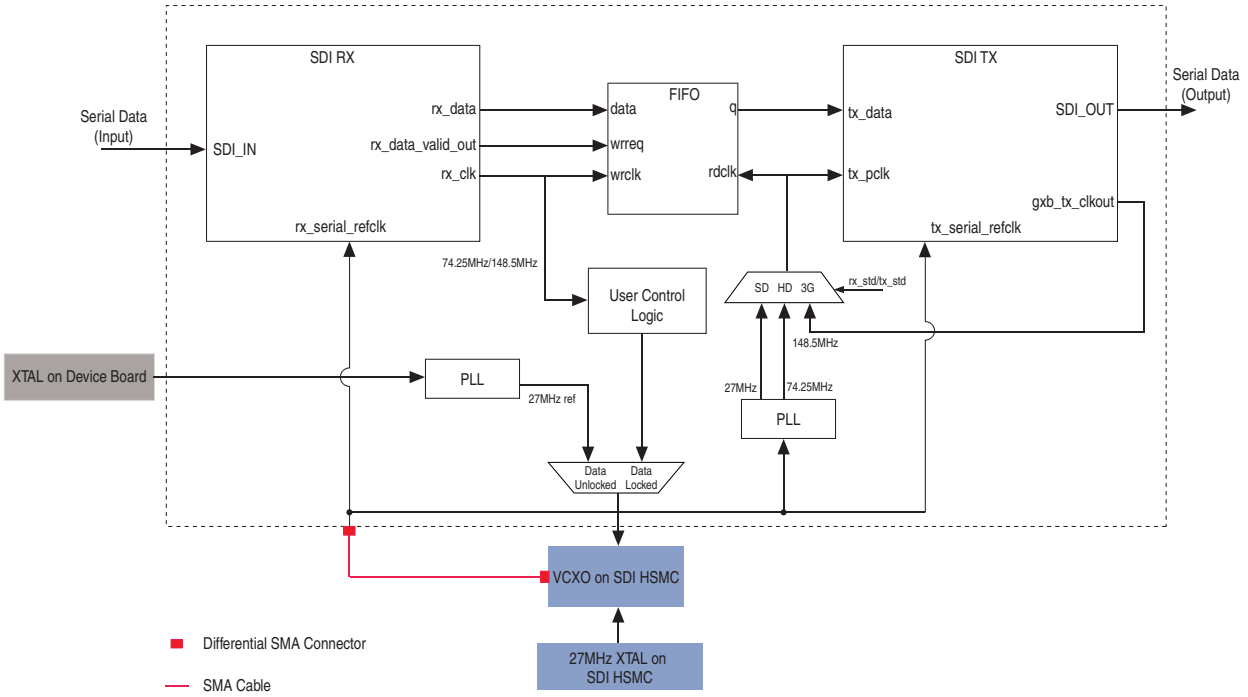
Voltage Controlled Crystal Oscillator (VCXO)

The VCXO device is a phase-locked loop (PLL) based synchronous clock generator (ICS810001) that is located on the SDI HSMC daughter card. This device contains two internal frequency multiplication stages that are cascaded in series.

The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation and to support the complex PLL multiplication ratios needed for video rate conversion. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency video output clock. The 148.5-MHz VCXO output clock is connected to the `rx_serial_ref_clk` and `tx_serial_ref_clk` clocks of the two SDI instances.

Figure 2 shows the block diagram for duplex loopback FIFO and the VXCO connection.

Figure 2. Duplex Loopback FIFO and VXCO Connection



Getting Started

This section discusses the requirements and how to run the reference design.

Hardware and Software Requirements

The demonstration requires the following hardware and software:

- Stratix V GX FPGA development kit or Arria V GX starter kit
- SDI HSMC
- Quartus® II software, version 12.0 SP1
- Two SMA cables

To obtain a Stratix V GX FPGA development kit or an Arria V GX starter kit, contact your local Altera representative.

Hardware Setup

Figure 3 and Figure 4 show how the Stratix V GX FPGA development board and the Arria V GX starter kit are connected to the SDI HSMC.

Figure 3. Stratix V GX FPGA Development Board with SDI HSMC

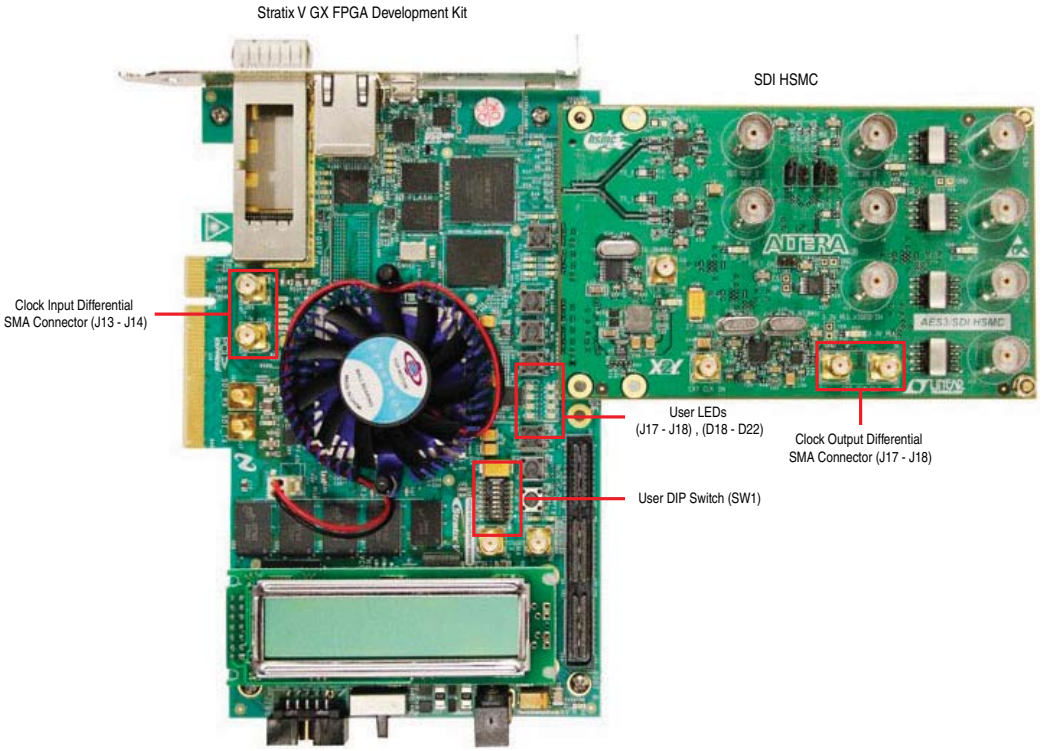


Figure 4. Arria V GX FPGA Starter Kit with SDI HSMC

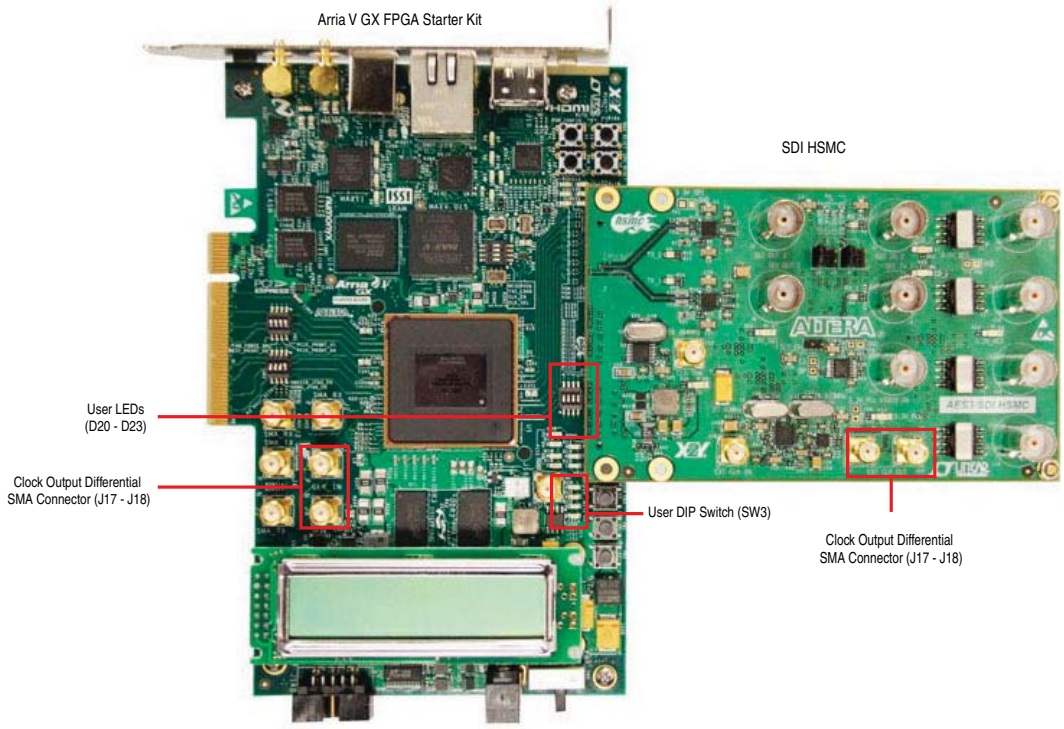


Table 1 describes the LED functions on the Stratix V GX development and Arria V GX starter kits.

Table 1. Functions of User LEDs (Part 1 of 2)

LED	Stratix V GX	Arria V GX	
		SW3.4 = "OFF"	SW3.4 = "ON"
D7	Internal pattern generator signal standard [D7, D8]: 00=SD, 01=HD, 11=3G	—	—
D8		—	—
D9	Clock out from transmitter (SDI TX)	—	—
D10	Clock out from receiver (SDI duplex)	—	—
D18	SDI IN 1 received signal standard [D18, D19] 00=SD, 01=HD, 11=3G	—	—
D19		—	—
D20	SDI IN 1 TRS Lock	Internal pattern generator signal standard [D7, D8]: 00=SD, 01=HD, 11=3G	SDI IN 1 received signal standard [D20, D1] 00=SD, 01=HD, 11=3G
D21	SDI IN 1 Frame Lock		

Table 1. Functions of User LEDs (Part 2 of 2)

LED	Stratix V GX	Arria V GX	
		SW3.4 = "OFF"	SW3.4 = "ON"
D22	—	Clock out from transmitter (SDI TX)	SDI IN 1 TRS Lock
D23	—	Clock out from receiver (SDI duplex)	SDI IN 1 Frame Lock

Table 2 describes the function of each board specific bi-color LED on the SDI HSMC.

Table 2. Board Specific Bi-Color LEDs

LED	Description
D1	SDI IN 2 receiving SDI signal in the following standards: ■ Green = 3G ■ Orange = HD ■ Red = SD
D3	SDI OUT 2 transmitting SDI signal in the following standards: ■ Green = 3G ■ Orange = HD ■ Red = SD
D5	SDI OUT 1 transmitting SDI signal in the following standards: ■ Green = 3G ■ Orange = HD ■ Red = SD
D6	SDI IN 1 receiving SDI signal in the following standards: ■ Green = 3G ■ Orange = HD ■ Red = SD

Table 3 describes the function of each user-defined DIP switch control.

Table 3. User DIP Switch Description (Part 1 of 2)

USER_DIP	Description	
	Stratix V GX (SW1)	Arria V GX (SW3)
7	Not used	—
6		—
5		—
4		—
3	1 = Select pathological SDI checkfield pattern 0 = Color bar	Refer to Table 1.

Table 3. User DIP Switch Description (Part 2 of 2)

USER_DIP	Description	
	Stratix V GX (SW1)	Arria V GX (SW3)
2	1 = 100% color bar 0 = 75% color bar	1 = Select pathological SDI checkfield pattern 0 = Color bar
1	Change internal pattern generator signal standard USER_DIP[1:0]: 00 = SD, 01 = HD, 11 = 3G	Change internal pattern generator signal standard USER_DIP[1:0]: 00 = SD, 01 = HD, 11 = 3G
0		

Table 4 describes the function of each push button.

Table 4. Reset Buttons

Push Button	Description	
	Stratix V GX	Arria V GX
PB0	Not used	1 = 100% color bar 0 = 75% color bar
PB1		Not used
PB2		

Running the Reference Design

To run the reference design follow these steps:

1. Set up the board connections.
   a. Connect the SDI HSMC to the FPGA development board.
   b. Specify the following board settings located on the back of the FPGA development board:
      - DIP switch bank
      - JTAG Chain Header Switch Controls
   c. Match the board settings to the settings in Table 5 and Table 6.
   d. Connect the FPGA development board to the power supply.
2. Download one of the following design examples, and save in your local:
   - s5gxsdi.qar (Stratix V GX)
   - a5gxsdi.qar (Arria V GX)
3. Launch the Quartus II software and click **s5gxsdi.qar** or **a5gxsdi.qar**.

Table 5. DIP Switch Control Settings

Switch	Schematic Signal Name	Description	Default
SW3 for Stratix V GX FPGA Development Kit			
1	CLK_SEL	ON: SMA input clock select OFF: Programmable oscillator input clock select (default 100MHz)	ON
2	CLK_ENABLE	ON: On-Board oscillator enabled OFF: O-Board oscillator disabled	ON
3	FACTORY_LOAD	ON: Load user 1 design from flash at power up OFF: Load factory design from flash at power up	ON
4	SECURITY_MODE	ON: Do not send FACTORY command at power-up OFF: Send FACTORY command at power-up	ON
SW2 for Arria V GX Starter Kit			
1	CLK_SEL	ON: Select SMA input clock OFF: Disable x1 presence detect	ON
2	CLK_ENABLE	ON: Disable On-board oscillator OFF: Enable On-board oscillator	OFF
3	FACTORY_LOAD	ON: Load the user design from flash at power up OFF: Load the factory design from flash for Arria V GX at power up	OFF
4	SECURITY_MODE	Reserve for future use	OFF

Table 6. JTAG Control DIP Switch Settings (Part 1 of 2)

Switch	Schematic Signal Name	Description	Default
SW3 for Stratix V GX FPGA Development Kit			
1	5M2210_JTAG_EN	ON: Bypass MAX V CPLD System Controller OFF: MAX V CPLD System Controller in-chain	OFF
2	HSMA_JTAG_EN	ON: Bypass HSMC port A OFF: HSMC port A in-chain	OFF
3	HSMB_JTAG_EN	ON: Bypass HSMC port B OFF: HSMC port B in-chain	ON
4	PCIE_JTAG_EN	ON: On-Board USB-Blaster II or external USB-Blaster is the chain master OFF: PCI Express edge connector is the chain master	ON
SW2 for Arria V GX Starter Kit			
1	5M2210_JTAG_EN	ON: Bypass MAX V CPLD 5M2210 System Controller OFF: MAX V CPLD 5M2210 System Controller in-chain	OFF

Table 6. JTAG Control DIP Switch Settings (Part 2 of 2)

Switch	Schematic Signal Name	Description	Default
2	HSMA_JTAG_EN	ON: Bypass HSMA OFF: HSMA in-chain	ON
3	PCIE_JTAG_EN	ON: Bypass PCI Express edge connector OFF: PCI Express edge connector in-chain	ON
4	NC	Not used	ON

4. Compile the reference design.
   a. On the File menu, click **Open Project**, navigate to **\<*directory*>\s5gxsdi.qpf** or **\<*directory*>\a5gxsdi.qpf**, and click **Open**.
   b. On the Processing menu, click **Start Compilation**.
5. Download the Quartus II-generated SRAM Object File (**.sof**), **\<*directory*>\s5gxsdi.sof** or **\<*directory*>\a5gxsdi.sof**.
   a. Connect the USB cable to the board's USB connector.
   b. On the Tools menu, click **Programmer** to download **\<*directory*>\s5gxsdi.sof** or **\<*directory*>\a5gxsdi.sof** to the board. The software automatically detects the file during compilation and it appears on the pop-up window**.**
   c. Click **Start** to download the file to the board. If the file does not appear in the pop-up window, click **Add File**, navigate to **\<*directory*>\s5gxsdi.sof** or **\<*directory*>\a5gxsdi.sof**, and click **Open**.

Reload each time after powering on the board because this design is volatile.

After setting up the board, run the different variants in the following sections.

Test Pattern Transmitter

To run the test pattern demonstration follow these steps:

1. Connect an SDI signal analyzer to the transmitter output of `SDI OUT2` (BNC J1). The LEDs indicate the following conditions:
   - LEDs D7, D8 (Stratix V GX) or D20, D21 (Arria V GX) indicate the internal pattern generator signal standard, which transmits through port 2 in the transmitter. Refer to Figure 5.

Figure 5. Condition of LEDs for Test Pattern Demonstration

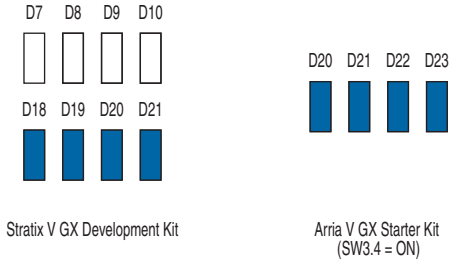
   - LED D5, on the SDI HSMC, illuminates to indicate the transmitter signal standard at port 1.
2. Check the result on the SDI signal analyzer.

Receiver

To run the receiver demonstration, follow these steps:

1. Connect an SDI signal generator to the receiver input of SDI IN1 (BNC J9) in Figure 6.
2. The receiver demonstration runs. The LEDs indicate the following conditions:
   - LEDs D18, D19 (Stratix V GX) or D20, D21 (Arria V GX) indicate the receiver signal standard.
   - LED D20 (Stratix V GX) or D22 (Arria V GX) illuminates when the received line format is stable at port 1.
   - LED D21 (Stratix V GX) or D23 (Arria V GX) illuminates when the receiver frame format is stable at port 1.

Figure 6. Condition of LEDs for Receiver Demonstration



Additionally, LED D6 on the SDI HSMC illuminates when the receiver signal standard is detected at port 1.

Serial Loopback

To run the serial loopback demonstration, follow these steps:

1. Connect transmitter output SDI OUT2 (BNC J1) to receiver input SDI IN1 (BNC J9).
2. The serial loopback demonstration runs. The LEDs indicate the following conditions:
   - LEDs D7, D8 (Stratix V GX) or D20, D21 (Arria V GX) indicate the internal pattern generator signal standard, which transmits through port 2 in the transmitter.
   - LEDs D18, D19 (Stratix V GX) or D20, D21 (Arria V GX) indicate the receiver signal standard.
   - LED D20 (Stratix V GX) or D22 (Arria V GX) illuminates when the received line format is stable at port 1.
   - LED D21 (Stratix V GX) or D23 (Arria V GX) illuminates when the receiver frame format is stable at port 1.

Figure 7. Condition of LEDs for Serial Loopback Demonstration

Additionally, the LEDs on the SDI HSMC indicate the following conditions:

- LED D5 illuminates when the transmitter signal standard is at port 1.
- LED D6 illuminates when the receiver signal standard is at port 1.

Parallel Loopback

To run the parallel loopback demonstration, perform the following steps:

1. Connect an SDI signal generator to the receiver input of `SDI IN 1`(BNC J9).
2. Connect an SDI signal analyzer to the transmitter output of `SDI OUT 1`(BNC J8).
3. The parallel loopback demonstration runs. The LEDs indicate the following conditions:
   - LEDs D18, D19 (Stratix V GX) or D20, D21 (Arria V GX) indicate the receiver signal standard.
   - LED D20 (Stratix V GX) or D22 (Arria V GX) illuminates when the received line format is stable at port 1.

- LED D21 (Stratix V GX) or D23 (Arria V GX) illuminates when the receiver frame format is stable at port 1.

Figure 8. Condition of LEDs for Parallel Loopback Demonstration

Additionally, the LEDs on the SDI HSMC indicate the following conditions:

- LED D6 illuminates when the receiver signal standard is at port 1.
- LED D3 illuminates when the transmitter signal standard is at port 1.

Document Revision History

Table 7 shows the revision history for this application note.

Table 7. Document Revision History

Date	Change Made	Summary of Changes
August 2012	1.0	Initial release