Implementing Clock Switchover in Stratix & Stratix GX Devices

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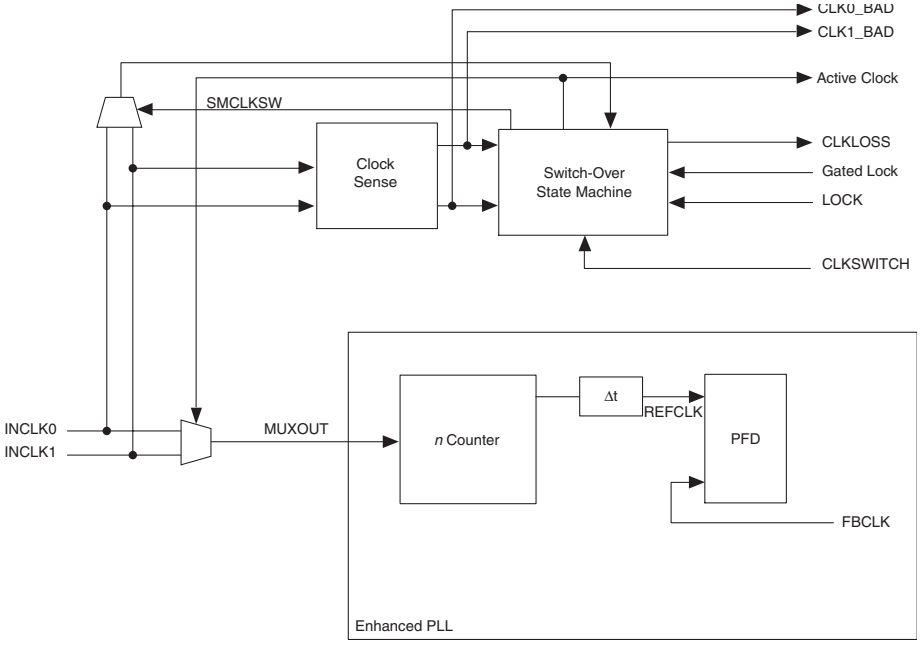
Introduction

The clock switchover feature allows the PLL to switch between two reference input clocks. Designers can use this feature for clock redundancy or for a dual clock domain application such as in a system where the system can turn on the redundant clock if the primary clock stops running. The clock switchover circuitry can perform clock switchover automatically, when the clock is no longer toggling, or based on a user control signal.

Clock Switchover

Stratix™ and Stratix GX device PLLs support a fully configurable clock switchover capability. Figure 1 shows the block diagram of the switchover circuit built into the enhanced PLL. The Stratix and Stratix GX devices fast PLLs do not support this feature. The major component of this circuitry is the clock sense block that automatically switches from primary to secondary clock for PLL reference when the primary clock signal is not present. The clock sense block can send out the `clk0_bad`, `clk1_bad`, and the `clk_loss` signals to LEs to implement a custom switchover circuit.

Figure 1. Clock Switchover Circuit Block Diagram



There are at least three possible ways to use the clock switchover feature.

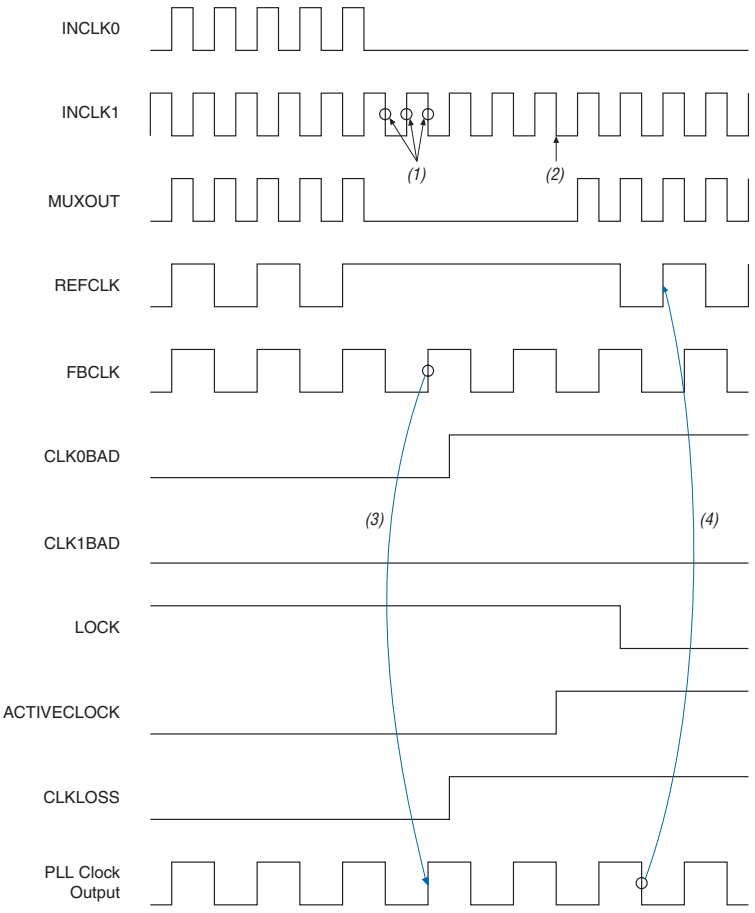
- Designers can use the switchover circuitry for switching from a primary to secondary clock of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 1. In this case, the secondary clock becomes the reference clock for the PLL. Automatic switchover can be used to switch from the primary to secondary clock only.

- Designers can use the clkswitch input for user- or system-controlled switchover conditions. This is possible for same-frequency switchover or to switch between clock inputs of different frequencies. For example, if extclk0 is 66 MHz and extclk1 is 100 MHz, the designer must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. Also, designers should choose the secondary clock frequency such that the VCO operates within the recommended range of 300 to 800 MHz. Designers can set the *m* and *n* counters accordingly to keep the VCO operating frequency in the recommended range. The gated lock circuit needs to be implemented in user logic.
- If the PLL loses lock for some reason, designers can implement a circuit in LEs gated lock to control switchover. The gated lock signal goes low to force the switchover state machine to switch to the secondary clock. If an external PLL is driving the Stratix or Stratix GX device PLL, excessive jitter on the clock input could cause the PLL to lose lock. Since the switchover circuit still senses clock edges, it might not sense a switch condition. In this case, the designer can control switchover using the gated version of the locked signal based on the loss of the primary clock.

Automatic Switchover

Figure 2 shows an example of a switchover feature waveform when using automatic clock loss detection. Here, the INCLK0 signal gets stuck low. After the INCLK1 signal gets stuck at low for approximately two clock cycles, the clock sense circuitry drives the clk0_bad signal high. Also, since the reference clock signal is not toggling, the clk_loss signal goes low indicating a switch condition. Then, the switchover state machine controls the multiplexer through the CLKSW signal to switch to the secondary clock.

Figure 2. Automatic Switchover Upon clkloss Detection



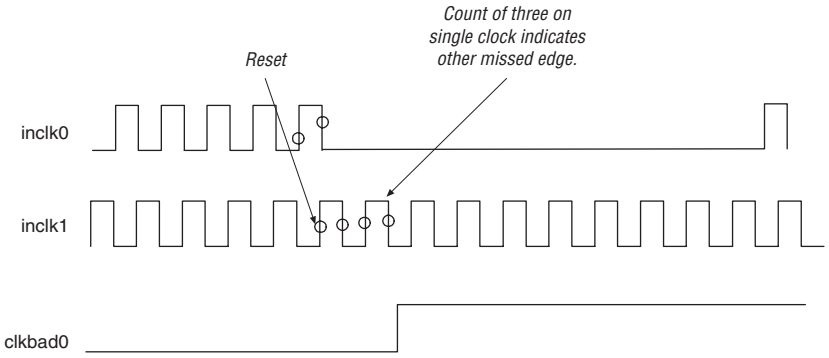
Notes to Figure 2:

(1) The number of clock edges before allowing switchover is determined by the counter setting.
(2) Switchover is enabled on the falling edge of `INCLK1`.
(3) The rising edge of `FBCLK` causes the VCO frequency to decrease.
(4) The rising edge of `REFCLK` starts the PLL lock process again, and the VCO frequency will increase.

The switchover state machine has two counters that count the edges of the primary and the secondary clocks. `counter0` counts the number of `inclk0` edges and `counter1` counts the number of `inclk1` edges. The counters get reset to zero when the count values reach 1,1; 1,2; 2,1; or 2,2 for `nclock0` and `nclock1`, respectively. For example, if `counter0` counts two edges, its count is set to two and if `counter1` counts two edges before the `counter0` sees another edge, they are both reset to 0. If

for some reason, one of the counters counts to 3, it means the other clock missed an edge. clkbad0 or clkbad1 goes high, and the switchover circuitry signals a switch condition. See Figure 3.

Figure 3. Clock-Edge Detection for Switchover



Manual Switchover

Figure 4 shows an example of a switchover feature waveform when controlled by clkswitch. In this case, both clock sources are functional and INCLK0 is selected as the primary clock. CLKSWITCH goes high, which starts the switchover sequence. On the falling edge of INCLK0, the reference clock to the *n* counter, MUXOUT, is gated off to prevent any clock glitching. On the falling edge of INCLK1, the reference clock multiplexer switches from INCLK0 to INCLK1 as the PLL reference. This is also the point the CLKSW signal changes to indicate which clock is selected as primary and which is secondary. The CLKLOSS signal mirrors the CLKSWITCH signal in this mode. Since both clocks are still functional during the manual switch, neither CLK_BAD signal goes high. Since the switchover circuit is edge-sensitive, the falling edge of the CLKSWITCH signal does not cause the circuit to switch back from INCLK1 to INCLK0. When the CLKSWITCH signal goes high again, the process repeats. CLKSWITCH and automatic switch will only work if the clock being switched to is available.

Figure 4. Clock Switchover Using the CLKSWITCH Control

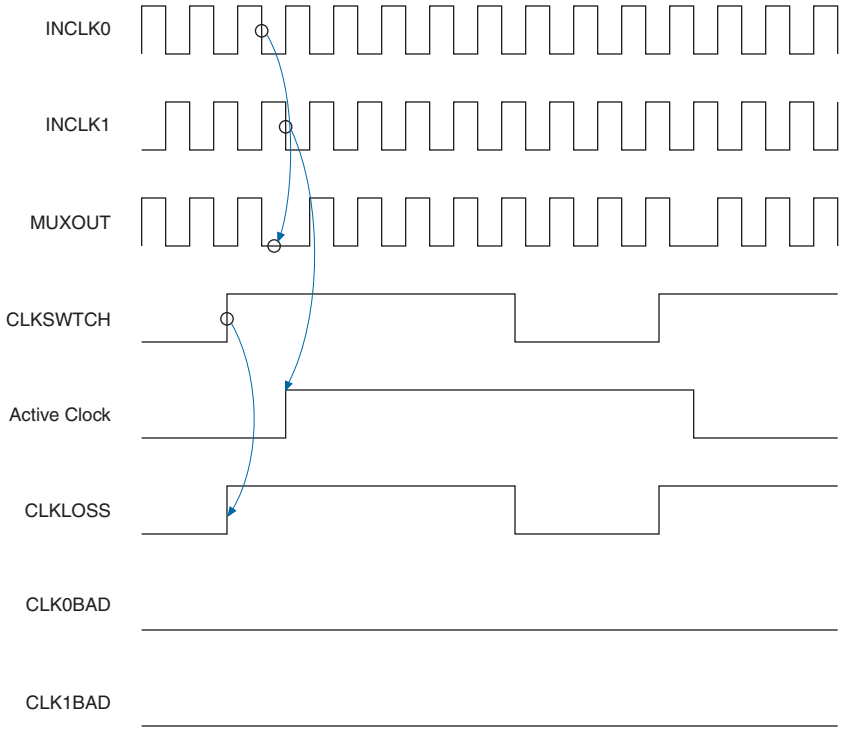
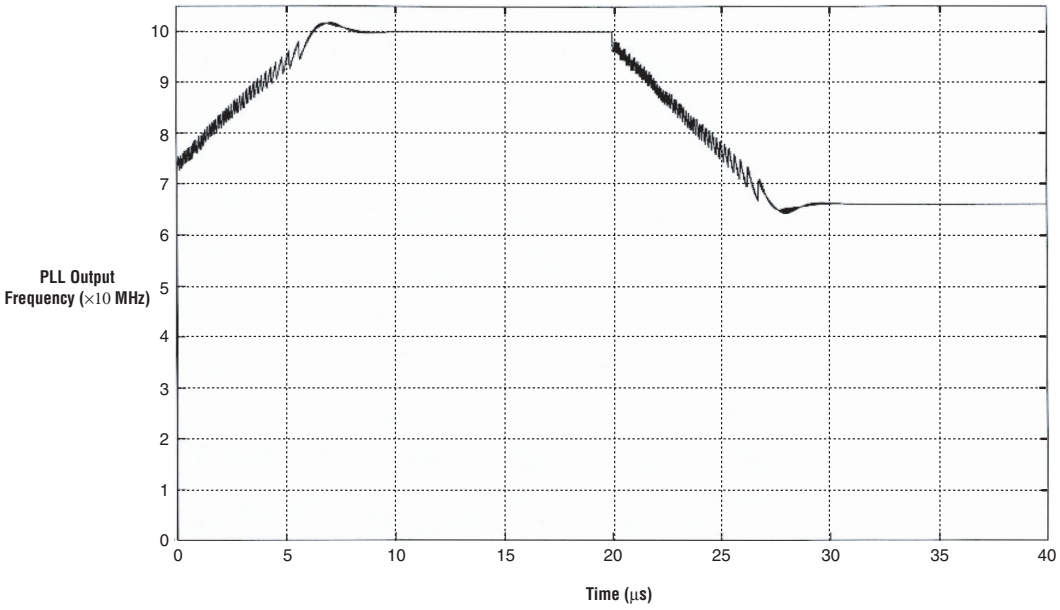


Figure 5 shows a simulation of using switchover for two different reference frequencies. In this example simulation, the reference clock is either 100 or 66 MHz. The PLL begins with f_{IN} = 100 MHz and is allowed to lock. At 20 µs, the clock is switched to the secondary clock, which runs at 66 MHz.

Figure 5. Switchover Simulation *Note (1)*



Note to Figure 5:

(1) This simulation was performed under the following conditions: the *n* counter is set to 2, the *m* counter is set to 16, and the output counter is set to 8. Therefore, the VCO operates at 800 MHz for the 100-MHz input and at 528 MHz for the 66-MHz reference input.

Lock-Signal-Based Switchover

The lock circuitry can initiate the automatic switchover. This is useful for cases where the input clock is still clocking, but its characteristics have changed so that the PLL is not locked to it. The switchover enable is based on both the gated and ungated lock signals. If the ungated lock is low, the switchover lock will not be enabled until the gated lock has reached its terminal count. The design will activate the switchover enable if the gated lock is high, but the ungated lock goes low. The switchover timing for this mode is similar to the waveform shown in Figure 4 for `CLKSWITCH` control, except the lock switchover enable replaces `CLKSWITCH`. Figure 6 shows the switchover enable circuit when controlled by lock and gated lock.

Figure 6. Switchover Enable Circuit

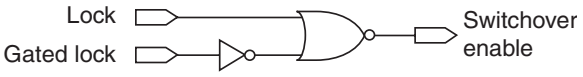


Table 1 summarizes the signals used for clock switchover.

Table 1. Clock Switchover Ports

Port	Description	Source	Destination
inclk0	Reference clk0 to the PLL	I/O pin	Clock switchover circuit
inclk1	Reference clk1 to the PLL	I/O pin	Clock switchover circuit
clkbad0	Signal indicating that refclk0 is no longer toggling	Clock switchover circuit	Logic array
clkbad1	Signal indicating that refclk1 is no longer toggling	Clock switchover circuit	Logic array
clkswitch	Switchover signal used to initiate clock switchover asynchronously	Logic array or I/O pin	Clock switchover circuit
clkloss	Signal indicating that the switchover circuit detected a switch condition clkloss = (! activeclock and clkbad0) or (activeclock and clkbad1) or (extswitch)	Clock switchover circuit	Logic array
locked	Signal indicating that the PLL has lost lock	PLL	Logic array
activeclock	Signal to indicate which clock (0 = inclk0 or 1 = inclik1) is driving the PLL	PLL	Logic array

Software Support

All the switchover ports shown in Table 1 are supported in the MegaWizard Plug-In Manager. The MegaWizard Plug-In Manager supports two methods for clock switchover:

- Automatic switchover, upon loss of the reference clock
- An internal user-controlled signal to trigger switchover

If the primary and secondary clock frequencies are different, the Quartus® II software will select the proper parameters to keep the VCO within the recommended frequency range.

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Guidelines

Use the following guidelines to design with clock switchover in PLLs.

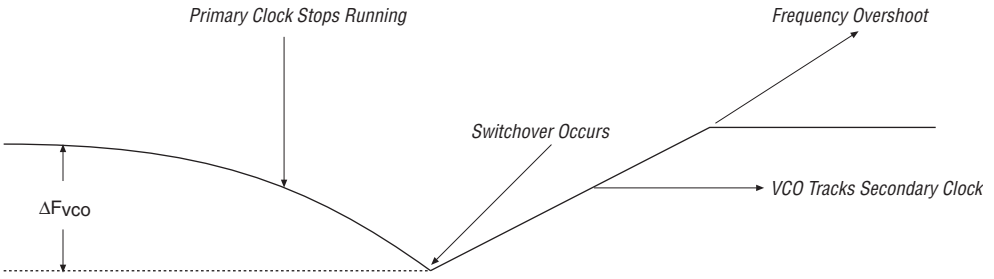
- The CLKSWITCH signal has a minimum pulse width that is based on the two reference clock periods. The CLKSWITCH pulse width must be greater than or equal to the period of the current reference clock (t_{from_clk}) multiplied by two plus the rounded up version of the ratio of the two reference clock periods. As an example, assume nominally t_{to_clk} is equal to t_{from_clk}. Then the CLKSWITCH pulse width should be at least three times the period of the clock pulse.

  $t_{EXTSWTCHmin} \geq t_{from\_clk} \times [2 + int_{round\_up} (t_{to\_clk}/t_{from\_clk})]$

- Applications that require a clock switchover feature and a small frequency drift should use a low-bandwidth PLL. The low-bandwidth PLL reacts slower than a high-bandwidth PLL to changes to its reference input clock. When the switchover happens, a low-bandwidth PLL propagates this stopping of the clock to the output slower than a high-bandwidth PLL. A low-bandwidth PLL filters out jitter on the reference clock. However, the trade-off is that the low-bandwidth PLL also increases lock time.
- Stratix device PLLs can use both the automatic clock switchover and the CLKSWITCH input simultaneously. Therefore, the switchover circuitry can automatically switch from the primary to the secondary clock, and once the primary clock stabilizes again, the CLKSWITCH signal can switch back to the primary clock. During switchover, the PLL VCO continues to run and will slow down, generating frequency drift on the PLL outputs. The CLKSWITCH signal controls switchover with its rising edge only.
- The clock switchover event is glitch-free. After the switch occurs, there is still a finite resynchronization period to lock onto a new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock is dependent on the PLL configuration. Designers can use the programmable bandwidth feature of the PLL to adjust the relock time.
- If the phase relationship between the input clock to the enhanced PLL and the input to the fast PLL is important in your design, assert ARESET for 10ns on the enhanced PLL after switching to the redundant clock. Wait for the enhanced PLL gated lock signal to go high before the enhanced PLL output clock is re-enabled.

- Figure 7 shows how the VCO frequency gradually decreases when the primary clock is lost and then increases as the VCO locks on to the secondary clock. After the VCO locks on to the secondary clock, there may be some overshoot (an over-frequency condition) in the VCO frequency.

Figure 7. VCO Switchover Operating Frequency



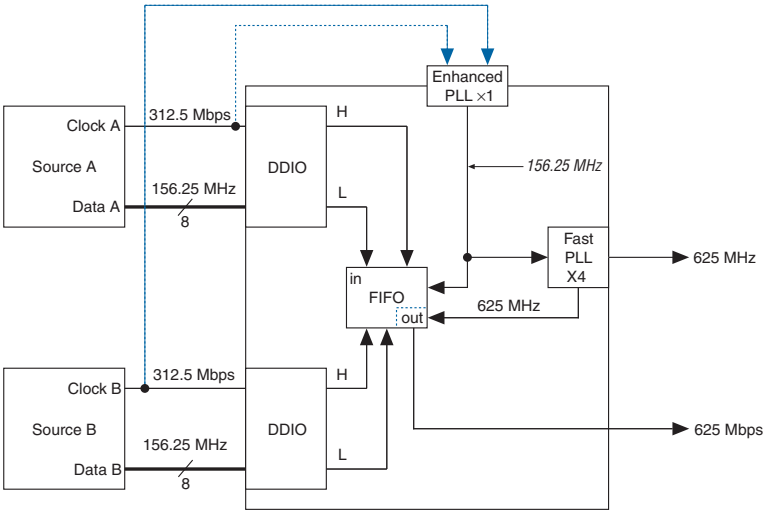
- Disable the system during switchover if it is not tolerant to frequency variations during the PLL resynchronization period. There are two ways to disable the system. First, the system may require some time to stop before switchover occurs. The switchover circuitry includes an optional five-bit counter to delay when the reference clock is switched. The designer can control the time-out setting on this counter (up to 32 cycles of latency) before the clock source switches. The designer can use these cycles for disaster recovery. The clock output frequency will vary slightly during those 32 cycles since the VCO can still drift without an input clock. Programmable bandwidth can control the PLL response to limit drift during this 32-cycle period.
- The second option available is to use the PFD enable signal (`pfdena`) along with user-defined control logic. In this case, the designer can use `clk0_bad` and `clk1_bad` status signals to turn off the PFD so the VCO maintains its last frequency. Designers can also use their own state machine to switch over to the secondary clock. Upon re-enabling the PFD, output clock enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clock(s).

For more information on a design issue affecting the `clk0_bad` and `clk1_bad` signals, see the *Stratix FPGA Errata Sheet*.

Clock Swithover Example Design

The clock switchover feature can be used to build a highly reliable redundant clocking system as shown in Figure 8. This system consists of a source synchronous interface (Source A) with a built in redundant source synchronous interface (Source B) to the Stratix device. The source-synchronous interface between each source and the Stratix device uses double data rate (DDR) signaling at 312.5 Mbps along with a 156.25-MHz clock. The redundant source synchronous interface is an exact replica of the source synchronous interface. The basic idea behind this design is to be able to switch to the redundant data and clock incase the primary source of the clock and/or data goes down or is corrupted.

Figure 8. Clock Switchover Example Design



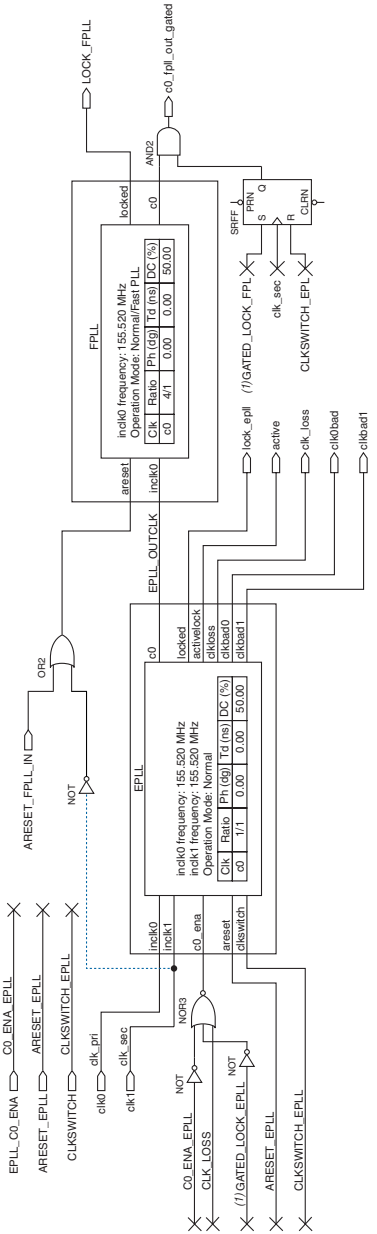
The enhanced PLL is fed by the primary clock from source A, and a secondary clock from the redundant source B interface. In turn, the enhanced PLL feeds one of these clocks to a Fast PLL which multiplies ×4 to output a 625-MHz clock. This high speed (625 MHz) clock is part of a 625-Mbps single data rate (SDR) LVDS interface with an off-chip serializer.

The Stratix device enhanced PLLs support clock switchover and hence form the front end of the design. The enhanced PLL can accept a primary clock source (clock A) as well as a secondary source (clock B) from the source A/B blocks. The 8-bit data from DataA and DataB are input through DDIO blocks and are monitored in internal logic to check for possible errors. An error flag goes high every time the error rate exceeds

a preset value. A multiplexer with the select line tied to the error flag can be used to switch between the data channel with the least number of errors introduced through this interface. The error flag also controls switching over to the corresponding clock for the data channel selected. Clock A corresponds to data A and clock B corresponds to data B.

Figure 9 shows the example design to implement the clock switchover feature in Stratix and Stratix GX devices. This design can be used as a starting point to build a design similar to Figure 8.

Figure 9. Implementing Clock Switchover *Note (1)*



Note to Figure 9:
(1) The gated lock circuits are not shown in this figure.

Design Implementation

The output clock from the enhanced PLL is enabled through the c0_ena port and is active as long as the following three criterions are met:

a. The CLKSWITCH signal is low

b. The LOCK output (gated) from the enhanced PLL is high

c. The optional input pin EPLL_C0_ENA is high

The output of the enhanced PLL feeds the fast PLL, which multiplies the 156.25-MHz input clock by four and outputs a 625-MHz clock to feed the serializer. During switchover, the CLK_LOSS signal goes high signaling a switch condition and this causes the output of the enhanced PLL to be gated off. Since the enhanced PLL output clock feeds the fast PLL, the rising edge of the CLKSWITCH will reset the fast PLL (output driven by ground) through the ARESET port of the PLL to guard against any possible glitching or frequency drift on the input to the fast PLL. The fast PLL is re-enabled only after the enhanced PLL has locked onto the secondary clock again.

If the phase relationship between the input clock to the enhanced PLL and the input to the fast PLL is important in your design, assert ARESET for 10 ns on the enhanced PLL after switching to the redundant clock. Wait for the enhanced PLL gated lock signal to go high before enabling the output clock from the enhanced PLL.

Design Simulation

Clock switchover can be initiated by asserting the CLKSWITCH and a zero-to-one (0 →1) transition on this signal causes the CLKLOSS signal to go high, which in turn disables the enhanced PLL output clock feeding the fast PLL. Since the input clock to the fast PLL is switched off, it is a good idea to reset the fast PLL by connecting the CLKLOSS signal from the enhanced PLL to the port of the fast PLL. Once the switchover is complete, the output clock from the enhanced PLL can be re-enabled and the fast PLL pulled out of reset so that it starts locking onto the enhanced PLL output clock.

Switchover Process

The following procedure directs the steps necessary for switchover:

1. The CLKSWITCH signal goes from 0 to 1.

2. The CLKLOSS signal goes high indicating a clock switch condition.

3. The c0_ena signal of the enhanced PLL is pulled low thereby disabling the enhanced PLL output clock.

4. The ARESET signal of the fast PLL is pulled high causing the fast PLL to be reset.

5. The CLKSWITCH signal goes from 1 to 0 signaling that the switchover process is complete.

6. The enhanced PLL output clock is re-enabled by pulling the c0_ena signal high.

7. The ARESET signal to the fast PLL is pulled low and the fast PLL is allowed to relock onto the enhanced PLL output clock.

If the phase relationship between the input clock to the enhanced PLL and the input to the fast PLL is important in your design, assert ARESET for 10ns on the enhanced PLL after switching to the redundant clock. Wait for the enhanced PLL gated lock signal to go high before the enhanced PLL output clock is re-enabled.

Conclusion

Clock switchover is a powerful feature that system designers can use to develop a highly reliable system in which the redundant clock can be switched on, in case the primary clock stops running for some reason. Clock switchover can be performed automatically, when the clock is no longer toggling, or based on a user control signal. These flexibilities offered by the Stratix device PLL make it a superior clock management system. Altera recommends that users follow the guidelines as described in this document when using this feature in their designs.

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