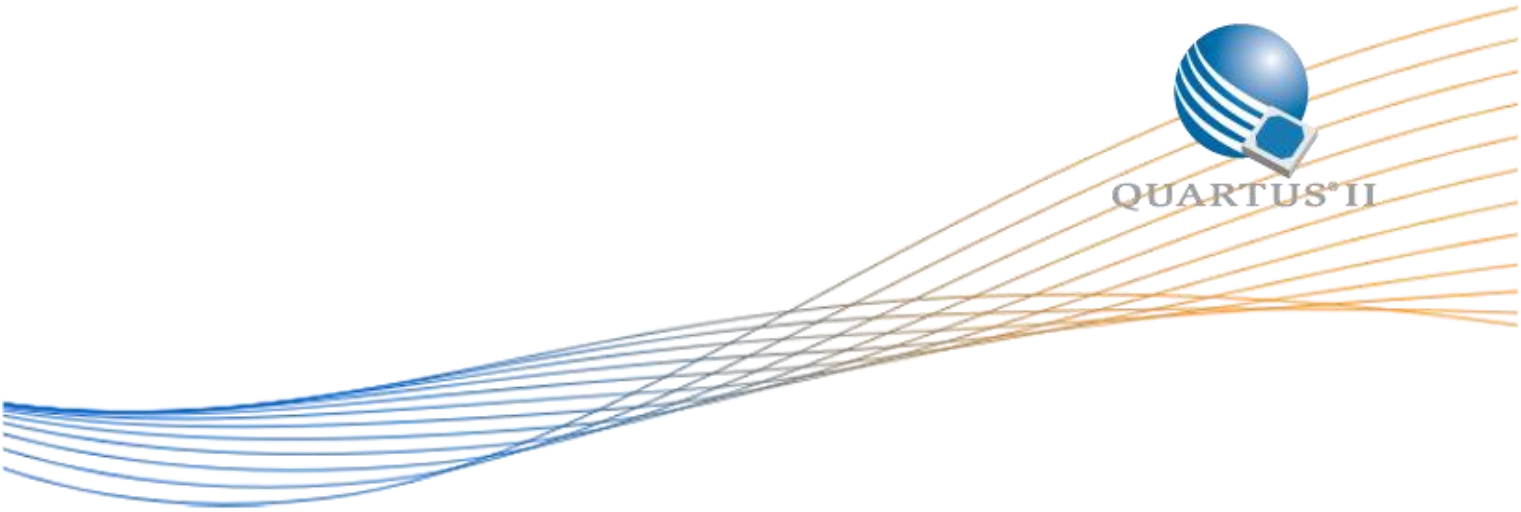

Arria 10 UHD Video Reference Design

Errata and Release Notes

Date: 01/02/2018

Revision: v3.0

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Introduction

This document accompanies the Arria 10 UHD Video Reference Design that is available from the Altera Design Store. It serves to alert the user to any errata or points of particular importance associated with this release of the design and is to be read in conjunction with the design's main documentation available as Application Note AN776.

This document accompanies v3.0 of the design.

NOTES

Note 1 – Terminal Display Messages

Unlike the last release, terminal message output feature can be switched on/off using the DIP switch setting (DIPSWITCH-SW2 number 8 controls the terminal message output).

When switched on NIOS II software running as part of the UHD Video Reference Design prints out status messages whenever changes are made to the scaling operation or when the output resolution changes. **Ensure that a "nios2-terminal" program is running in order for these messages to be displayed.**

NOTE: if a nios2-terminal is not running, there is a likelihood that the NIOS II will block whilst attempting to print out messages and the design will stop responding to any key presses or input source changes.

To alter the NIOS II software as supplied with the UHD Video Reference Design to remove the messages and hence the dependency on the nios2-terminal, edit line 5 in the file main.cpp in the software/vip_control_src directory to be:

```
#define VERBOSE    0
```

Follow the instructions in the Application Note as to how to recompile the NIOS II software.

Errata

Errata 1 – IOPLL Issues

There is a known issue in the Quartus compile process regarding the connectivity of IOPLLs for some designs. This issue can lead to the misconfiguration of the IOPLLs causing design malfunction. There is a workaround for this problem in Quartus 16.1 with a fix planned in Quartus 18.0.

The workaround as used in the current version of the UHD Video Reference Design (since this version uses Quartus 17.1) is to enable the following setting in the quartus.ini file:

pcc_use_a2c_for_rotation=off

Errata 2 – Quartus Timing Violations

There is a known issue in the Clocked Video Input II (CVI II) block that causes recovery timing violations to be reported. These timing violations are associated with the reset signal used as input to a clock crossing synchronizer interface between the two clocks in the CVI II and don't cause any functional problems. The first clock is video input clock from the HDMI Rx; the second is the clock used by the video pipeline (VIP_CLK). It is this first clock, named "u_hdmi_rx_top|u_iopll|pll_hdmi|outclk2", against which the timing violations are reported.

This issue is fixed in the 17.1.1 for Pro (and in 18.0 for Std version of Quartus).

Quartus Critical Warnings

Critical Warning 1

Critical Warning (127005): Memory depth (16) in the design file differs from memory depth (10) in the Memory Initialization File "<pat> /top.ram0_mr_rom_rx_dprioaddr_bitmask_96c28190.hdl.mif" -- setting initial value for remaining addresses to 0

The MIF file referred to here only requires 10 entries whereas the matching physical RAM has the required number of entries as a power of two, hence the mismatch.

Revision History

Date	Version	changes
2016 August 19	1.0	Intial release
2016 August 22	1.1	Wording of IOPLL errata
2017 November 1	3.0	17.0 release note
2018 January 2	3.0	17.1 Pro release note